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Audit Report

OFFICE OF THE INSPECTOR GENERAL

MICROELECTRONICS CHIP MANUFACTURING

Report No. 95-164 April 3, 1995

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Acronyms

ALC	Air Logistics Center
ASIC	Application Specific Integrated Circuits
MMST	Microelectronic Manufacturing Science and Technology
NSA	National Security Agency
SPL	Special Processing Laboratory

INSPECTOR GENERAL
DEPARTMENT OF DEFENSE
400 ARMY NAVY DRIVE
ARLINGTON, VIRGINIA 22202-2884

Report No. 95-164 April 3, 1995

MEMORANDUM FOR ASSISTANT SECRETARY OF THE AIR FORCE
(FINANCIAL MANAGEMENT AND COMPTROLLER)
DIRECTOR, NATIONAL SECURITY AGENCY/CHIEF,
CENTRAL SECURITY SERVICE

SUBJECT: Audit Report on Microelectronics Chip Manufacturing
(Project No. 3RC-0026)

We are providing this report for your review and comments. The report discusses DoD's microelectronics chip manufacturing requirements and capabilities. Comments on a draft of this report were considered in preparing this final report.

DoD Directive 7650.3 requires that all audit recommendations be resolved promptly. The Air Force disagreed with terminating the contract for the enhancement for the Microelectronic Manufacturing Science and Technology Program. The Air Force must provide final comments on the unresolved recommendation and potential monetary benefits by May 31, 1995. See the end of Finding B for a discussion of the specific requirements for your response.

The courtesies extended to the audit staff are appreciated. If you have any questions on this audit, please contact DoD OIG (b)(6), Audit Program Director, at DoD OIG (b)(6) (DSN DoD OIG (b)(6)) or DoD OIG (b)(6), Audit Project Manager, at DoD OIG (b)(6). The distribution of this report is listed in Appendix H. The audit team members are listed inside the back cover.

Robert J. Lieberman
Assistant Inspector General
for Auditing

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Office of the Inspector General, DoD

Report No. 95-164 **April 3, 1995**
(Project No. 3RC-0026)

MICROELECTRONICS CHIP MANUFACTURING

EXECUTIVE SUMMARY

Introduction. Department of Defense weapons and intelligence systems are dependent on microelectronics components. Current microelectronics technology allows thousands of circuits to be printed on a single chip for high-speed signal processing. In 1985, the National Security Agency (NSA) built a microelectronics chip manufacturing facility to satisfy requirements for classified chips that could not be obtained from commercial sources.

In September 1988, the Advanced Research Projects Agency and the Air Force initiated the Microelectronic Manufacturing Science and Technology (MMST) Program. The objective of the MMST Program was to demonstrate concepts for the flexible, cost-effective, low-volume manufacture of application-specific integrated circuits. The initial portion of the MMST Program was completed in June 1993 at a cost of $86 million. However, the Air Force plans a modification costing $7.4 million.

Objectives. The overall audit objective was to evaluate DoD's microelectronics chip manufacturing requirements and capabilities. The audit included an evaluation of the effectiveness and efficiency of operations at the NSA Special Processing Laboratory. The audit also answered a congressional inquiry, received during the audit, concerning the purchase of equipment NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) for the Special Processing Laboratory. In addition, the audit evaluated the implementation of the NSA's internal management control program and assessed the adequacy of internal controls related to the overall objective.

Audit Results. The Military Departments' microelectronics chip manufacturing capabilities (see Appendix E) are sufficient to satisfy the Military Departments' requirements. NSA (b)(3) 50 USC 3605 [redacted] (Finding A). Further, the Air Force was planning an unneeded modification at a cost of $7.4 million to the MMST Program (Finding B).

NSA's purchases of material for the Special Processing Laboratory NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) [redacted] complied with the Defense Federal Acquisition Regulation Supplement (see Part I, Other Matters of Interest).

Potential Benefits of the Audit. Implementation of the recommendations will allow the Air Force to put to better use $7.4 million in research, development, test and evaluation funds. Appendix F summarizes all potential benefits of this audit.

Summary of Recommendations. We recommend that the Director, National Security Agency, determine whether the Special Processing Laboratory can manufacture unclassified microelectronics chips NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) [redacted] We also recommend that the Director, Wright Laboratory, cancel the modification to the MMST contract.

Management Comments. NSA indicated that a complete review of its acquisition policy was needed before a definitive policy on manufacturing unclassified microelectronics chips at the Special Processing Laboratory could be enacted. The review will be completed by May 25, 1995.

The Air Force disagreed with cancelling the modification to the MMST contract and stated that the dissemination of MMST technology throughout the semiconductor industry provides sufficient benefits to DoD to justify continuation of the MMST program. See Part I for a complete discussion of management comments and Part III for the complete texts of management comments.

Audit Response NSA's comments are responsive. We do not agree with the Air Force position that the benefits derived by the U.S. semiconductor industry from the MMST Program justify its continuation. Therefore, we ask that the Air Force reconsider its position and provide comments on the final report by June 2, 1995.

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Part I - Introduction

Background

Microelectronic Chips. The proliferation of all types of microelectronics components for DoD weapons systems created a requirement for DoD to remain active in the microelectronics arena. A microelectronics chip (also known as a die) is a single square or rectangular piece of semiconductor material into which a specific electrical circuit has been fabricated. Microelectronics chips are also known as integrated circuits. An integrated circuit is an electronic circuit made by fabricating components, such as resistors, capacitors, and transistors, onto a single piece[1] of semiconductor material, usually silicon. Current microelectronics technology allows thousands of circuits to be placed on a single chip for high-speed signal processing. Chips can be designed to accomplish a general task, such as a processor does in a computer, or to accomplish a specific task or function, such as performing a complex mathematical formula. Chips designed for a single function are referred to as Application Specific Integrated Circuits (ASICs).[2]

Microelectronic Chip Manufacturing Facilities. Chip manufacturers use generally large volume, mass-production type factories to produce microelectronics chips. The cost to build chip manufacturing facilities ranges from $175 million to $1 billion, depending on size. A facility can become technologically obsolete in about 3 years. Chip manufacturing facilities produce 0.8 to 1.0 micron size chips on silicon wafers, with usually 30 to 40 chips on a wafer. Wafers are processed in batches of 25 to 50 and take 30 to 90 days to complete.

Special Processing Laboratory. In FY 1983, the National Security Agency (NSA) identified a requirement for an in-house manufacturing facility, the Special Processing Laboratory (SPL), to produce classified ASICs. NSA established the requirement for the SPL because commercial firms able to manufacture and deliver high-quality ASICs did not want to comply with NSA's security requirements and delivery schedules. NSA initiated construction of the SPL in 1986 and completed it in 1990. The National Semiconductor Corporation operated the SPL until January 1991 when NSA assumed operational control.

Microelectronic Manufacturing Science and Technology Development. In September 1988, the Advanced Research Projects Agency and the Air Force, at Wright Laboratory, initiated a program to demonstrate

[1]Commonly referred to as a wafer.

[2]A glossary in Appendix A defines microelectronics chip manufacturing terms.

concepts for the flexible, cost-effective, low-volume manufacture of ASICs. Wright Laboratory, Department of the Air Force; Advanced Research Projects Agency; and Texas Instruments, Incorporated (Texas Instruments), entered into an agreement to start the Microelectronic Manufacturing Science and Technology (MMST) Program. The initial cost-share contract was valued at $112.6 million.

Objectives

The overall audit objective was to evaluate DoD's microelectronics chip manufacturing requirements and capabilities. The audit included an evaluation of the effectiveness and efficiency of operations at the SPL and answered a congressional inquiry, received during the audit, concerning the purchase of material for the SPL NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) (see Other Matters of Interest). The audit also evaluated the implementation of the NSA internal management control program and assessed the adequacy of internal controls applicable to the overall audit objective.

Scope and Methodology

DoD Microelectronics Chip Manufacturing Capabilities. To assess DoD's microelectronics chip manufacturing capabilities, we:

o interviewed cognizant Government officials responsible for microelectronics research and engineering,

o discussed DoD and industry chip manufacturing capabilities with officials of the Semiconductor Manufacturing Technology Consortium (Consortium),[3]

o visited and toured the facilities of DoD organizations that had microelectronics chip manufacturing capabilities, and

[3]A consortium of American Semiconductor Manufacturers working with the U.S Government to sponsor research aimed at assuring global leadership for the U.S semiconductor industry.

o reviewed those DoD organizations' missions and functions statements, budget plans, capital investment funding requests, and other documentation related to their operations.

Purchases of Application Specific Integrated Circuits. To determine the DoD requirements for ASIC chips, we reviewed DoD contracts with chip manufacturers and used statistical sampling techniques to determine the number of ASIC chips purchased during FY 1993. We randomly selected and reviewed 366 of 6,172 contract actions with chip manufacturers. The 366 contract actions were issued by DoD procurement organizations in 12 states. The Audit Planning and Technical Support Directorate, Office of the Assistant Inspector General for Auditing, DoD, provided technical assistance in helping the auditors formulate the statistical sampling plan.

Special Processing Laboratory Operations. To determine the effectiveness and the efficiency of the SPL operations, we reviewed:

o the SPL's operational support contract, related modifications, and monthly management status reports;

o SPL reports on classified and unclassified ASIC chip requirements, production, and deliveries; and

o the January 1983 justification, DD Form 1391, submitted to Congress for the construction of the SPL.

We interviewed NSA personnel responsible for contract administration and oversight of SPL operations and Consortium personnel regarding NSA's purchase of equipment NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) to support SPL operations. In addition, we examined the SPL's long-range funding requirements for FY 1993 through FY 1998 and NSA's contracts with ASIC chip manufacturers for FY 1992 and FY 1993.

Microelectronic Manufacturing Science and Technology Program. To determine the effectiveness of the management of the MMST development, we reviewed memorandums of understanding between the Advanced Research Projects Agency and Wright Laboratory on MMST objectives and responsibilities, the MMST contract and contract modifications, minutes of MMST program review meetings, and project files dated from July 1987 through June 1993.

Computer-Processed Data. We extracted information on DoD contracts with chip manufacturers from the FY 1993 DD350 Individual Contracting Action Report data base maintained by the Procurement and Economics Information Division, Washington Headquarters Services Center. We did not assess the accuracy of the DD350 data base because we used the information only to

determine whether DoD had purchased ASIC chips. Also, we extracted NSA contracts and purchases for SPL operations from NSA's [redacted] data bases. We used that information only to assess contract purchases and job operations at the SPL. Inaccuracies in the data bases we accessed will not affect the results of the audit or the report recommendations.

Audit Period and Standards. This economy and efficiency audit was made from February 1, 1993, through March 31, 1994, in accordance with auditing standards issued by the Comptroller General of the United States, as implemented by the Inspector General, DoD. Accordingly, we included tests of internal controls as were considered necessary. The organizations we visited or contacted are listed in Appendix G.

Internal Controls

Internal Controls Reviewed. We reviewed internal controls related to the validation of requirements for ASIC chips and the procedures used to document requirements for facilities manufacturing microelectronics chips. Also, we assessed the implementation of NSA's internal management control program applicable to the operation of the SPL, and we assessed Wright Laboratory's internal management control program applicable to processing contract modifications.

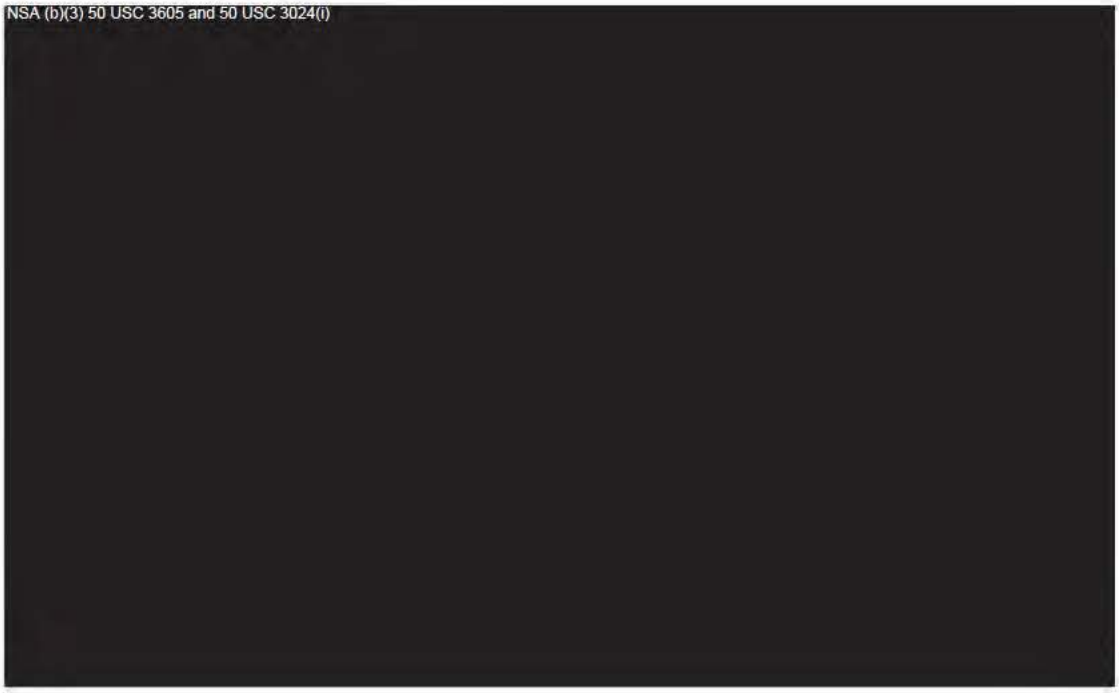
Adequacy of Internal Controls. The audit identified no material internal control weaknesses as defined by DoD Directive 5010.38, "Internal Management Control Program," April 14, 1987, in either NSA's or Wright Laboratory's internal management control programs. However, Wright Laboratory personnel had not followed procedures for determining whether requirements that had been previously validated were still current. Details are in Finding B, Part II.

Prior Audits and Other Reviews

Two Inspector General, DoD, reports on issues related to microelectronic chip manufacturing have been issued. Report No. 94-195, "Pay Differentials at the NSA's Microelectronic Facilities," September 23, 1994, reported that NSA was making unnecessary payments for hazard and environmental pay differentials. The report recommended modifying procedures for authorizing pay differentials and terminating pay differentials to put [redacted] to better use annually. The Director, National Security Agency, agreed to the recommended actions and

indicated that monetary benefits will be achieved. Report No. 95-008, "Microelectronic Manufacturing Science and Technology Program" October 12, 1994, reported that Wright Laboratory personnel did not effectively safeguard technology developed under the MMST program. The Air Force agreed to strengthen its procedures to control technology transfers. The executive summaries for those reports are in Appendixes B and C.

Other Matters of Interest



Part II - Findings and Recommendations

Finding A. Special Processing Laboratory Utilization

The National Security Agency is not fully utilizing its Special Processing Laboratory. Underutilization occurred because NSA managers had not considered the SPL production of unclassified chips as an alternative to obtaining the chips from commercial sources. NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

ASIC Chip Requirements

NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

Special Processing Laboratory

Construction of the Special Processing Laboratory. The SPL provides NSA an in-house capability to produce classified ASICs for NSA and other members of the intelligence community. Construction of the SPL began in 1986 and was completed in 1990. The construction and installation of the manufacturing equipment cost about $125 million. In January 1991, the SPL became fully operational and began to produce ASICs. The Microelectronics Division of NSA's Technology and Systems Organization is responsible for the operation of the SPL.

Manufacturing Capabilities. The ASIC production line is inside a 20,000-square-foot, class 10 clean room. The National Semiconductor Corporation equips the SPL and provides manufacturing technology. The SPL manufactures ASICs on 6-inch silicon wafers using three National

Semiconductor Corporation processes NSA (b)(3) 50 USC 3605 [redacted] ASIC production in the SPL involves a four-stage process: maskmaking, wafer fabrication, assembly, and testing. Appendix D provides details on the production process.

SPL Work Load

NSA (b)(3) 50 USC 3605 [redacted]

Manufacturing Capacity

Special Processing Laboratory Manufacturing Capacity. The SPL's capacity for manufacturing ASIC chips is dependent on the maskmaking, wafer fabrication, and assembly shops. The testing shop does not affect the SPL's manufacturing capacity. The wafer fabrication and the assembly shops are the two main production areas of the SPL and are responsible for the ASIC chip manufacturing and packaging, respectively.

Maskmaking Operations. NSA (b)(3) 50 USC 3605 [redacted]

NSA (b)(3) 50 USC 3605

[redacted]

Wafer Fabrication. NSA (b)(3) 50 USC 3605

[redacted]

Finding A. Special Processing Laboratory Utilization

NSA (b)(3) 50 USC 3605

[redacted]

Assembly Operations. NSA (b)(3) 50 USC 3605

[redacted]

NSA (b)(3) 50 USC 3605

NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

Finding A. Special Processing Laboratory Utilization

NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

[redacted]

[4]A Class B chip is a microelectronics chip that must pass stringent stress and environmental tests to meet a specified reliability standard for all applications except outer space applications.

NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

[redacted]

Recommendation, Management Comments, and Audit Response

A. We recommend that the Director, National Security Agency/Chief, Central Security Service, determine whether the Special Processing Laboratory can produce unclassified microelectronics chips NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) [redacted].

Management Comments. The National Security Agency stated that a complete review of its acquisition policy was needed before a definitive policy on manufacturing unclassified microelectronics chips at the SPL could be enacted. The planned completion date for that review is May 25, 1995. See Part IV for the complete text of the comments.

Audit Response. The planned review satisfies the intent of the recommendation.

Finding B. Microelectronic Manufacturing Science and Technology Program

The Air Force is planning an unneeded modification to the MMST contract, although DoD organizations have not demonstrated a need for the MMST technology already developed. Planning for the modification continues because the program office did not verify whether the requirement was still valid. Consequently, the Air Force could spend $7.4 million unnecessarily.

Background

Goals and Objectives. The Advanced Research Projects Agency and the Air Force Manufacturing Technology Directorate, Wright Laboratory, established the MMST Program in 1988 to demonstrate concepts for cost-effective, flexible, low-volume manufacture of ASICs. The MMST Program focused on DoD's need for access to a low-volume, ASIC production facility. The Advanced Research Projects Agency characterized the MMST Program as a revolutionary concept for flexible semiconductor manufacturing. Successful completion of the MMST endeavor would provide DoD access to an affordable manufacturing technology and would provide U.S. microelectronic chip manufacturers a highly flexible, automated manufacturing capability. The Advanced Research Projects Agency and the Air Force projected that an MMST facility would cost about $30 million, once the MMST concept had been demonstrated. The production cost for the MMST would be significantly below the $175 million cost of a traditional chip manufacturing facility. In 1988, personnel at the MMST project management office at Wright Laboratory identified the Sacramento Air Logistics Center (ALC), McClellan Air Force Base, California; the Ogden ALC, Hill Air Force Base, Utah; and the NSA as DoD organizations that were considering the purchase of MMST facilities once the program was completed.

Cost Sharing and Project Modification. Texas Instruments, Incorporated (Texas Instruments), agreed to absorb 32 percent of the development cost for the MMST Program. Wright Laboratory awarded a cost-share contract, valued at $112.6 million, to Texas Instruments in September 1988. In May 1991, Wright Laboratory modified the contract requirements, reducing the value to $86 million. In May 1993, contract costs totaled $96.9 million when Wright Laboratory personnel modified the contract and increased the value by $10.9 million. Wright Laboratory's share of the increase was $7.4 million and

Texas Instrument's share was $3.5 million. The modification added a Cluster Tool Process Enhancement task to the MMST contract. The Cluster Tool Process Enhancement task is to develop a dry cleanup process and a silicon-on-insulator process flow. The silicon-on-insulator process will facilitate the manufacture of complex radiation-hardened chips. Wright Laboratory project managers did not determine whether the organizations identified in 1988 were still interested in the MMST Program when the managers initiated the modification.

MMST Accomplishments

The MMST Program has been recognized as a significant accomplishment in enhancing low-volume integrated circuit manufacturing capabilities. Personnel at the Consortium indicated that many American companies are using MMST concepts in the development of rapid thermal processing applications. Consortium personnel believe that the MMST technology will be used extensively in chip manufacturing production facilities in the future. Further, the software developed for production planning, scheduling, material handling, and tracking developed as part of the MMST Program is being used by the Consortium in developing standards for industry-wide use.

DoD Requirement for MMST Facilities

MMST Procurements. Although MMST technology is providing a technical base for use by microelectronics equipment manufacturers, none of the DoD organizations identified by the MMST program office in 1988 are planning to procure MMST facilities. See Appendix E for a discussion of DoD's microelectronics chip manufacturing capabilities.

Sacramento-ALC Requirements. Sacramento-ALC requested funds to purchase an MMST facility in FY 1993. Sacramento-ALC applied for funds under the provisions of the Defense Production Act program (referred to as Title III). DoD's Title III program office disapproved the funding request, because Sacramento-ALC could not demonstrate that it would be cost-effective to purchase an MMST facility. Sacramento-ALC personnel did not know how many chips they would produce in an MMST facility on a yearly basis or the annual operating costs of the facility. Further, the MMST program office had not identified the annual cost of operating an MMST facility. Sacramento-ALC procurements made during FY 1993 showed that about 200 ASIC chips had been procured at a cost of $250,000. MMST program office personnel

projected that a fully operational MMST facility could produce 50,000 chips annually. Consequently, Sacramento-ALC does not have sufficient requirements for an MMST chip manufacturing facility.

Ogden-ALC Requirements. Ogden-ALC considered procuring an MMST facility to support its mission of repairing electronic components. Ogden-ALC personnel believed that it might be more cost-effective to design ASIC chips to replace older components that were no longer available through supply sources. However, the personnel determined that a different type of chip, the Field Programmable Gate Array, provided a more cost-effective alternative. The average cost of a Field Programmable Gate Array is about $200. Ogden-ALC purchased about 2,000 Field Programmable Gate Arrays during FY 1993 at a cost of about $400,000. Since the projected cost of an MMST was about $30 million, Ogden-ALC personnel did not give further consideration to procuring an MMST facility.

National Security Agency Requirements. Personnel in NSA's SPL stated that they had attended conferences on the MMST Program during the early stage of its development. SPL personnel were interested in the MMST Program's goals and objectives. However, since NSA contracted with National Semiconductor Corporation to obtain manufacturing technology, SPL personnel did not further consider procuring an MMST facility.

Other DoD Component Requirements. No other DoD Component had requirements for the MMST Program. Personnel at the Army's Electronic and Power Sources Directorate, Army Research Laboratory, indicated that the Army had no requirement for the MMST technology or for an MMST facility. Personnel at the Navy's Electronics Science and Technology Division responded similarly regarding the Navy's requirements.

Microelectronics Chip Requirements. DoD organizations were not purchasing ASICs directly from chip manufacturers. Based on our statistical sample, we estimated that fewer than 8,000 ASIC chips were purchased during FY 1993. NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) Other DoD organizations procured circuit boards with the chips attached. The numbers and types of the chips on the circuit boards were not usually known to the ordering organization.

Radiation Hardened Chips

No DoD organization demonstrated a requirement for a capability to produce small quantities of radiation hardened chips. Radiation hardened chips are generally used in missiles and satellites that will have to operate in space with

exposure to high dosages of radiation. We discussed the requirement for radiation hardened chips with Army and Air Force personnel responsible for the missile and space programs. Their primary contractors provided the needed chips. The Army and Air Force had not experienced problems in obtaining sufficient quantities of repair parts. Also, the Department of Energy has the capability to produce limited quantities of radiation hardened chips at its Sandia Laboratory. The Sandia Laboratory has supported several DoD programs, including the Trident Missile program and the Strategic Defense Initiative. Further, the Consortium initiated research into the production of silicon-on-insulator chips that could meet requirements for radiation hardened chips. Because the DoD organizations have expressed no need for the silicon-on-insulator process, the Cluster Tool Process Enhancement for the MMST contract is not needed.

Modification Status as of October 30, 1994

Although the MMST contract was modified in May 1993 to allow work on the Cluster Tool Process Enhancement modification, work had not commenced as of October 30, 1994. Wright Laboratory issued a stop work order in November 1993. The stop work order was issued because Congress cut DoD's Manufacturing Technology Program budget in FY 1994. Because of the congressional action, 23 of 45 manufacturing technology projects at Wright Laboratory were stopped. However, managers at Wright Laboratory plan to use $7.4 million of the laboratory's FY 1995 through FY 1998 budget to complete the MMST Program.

Program Continuation

Continuation of the MMST Program is not warranted. Although building an MMST facility is less costly than building a mass production facility, only NSA has demonstrated a requirement for the MMST program. Because NSA already has a facility that is underutilized, developing additional capabilities is unnecessary. Further, DoD's requirement for radiation hardened chips was sufficiently satisfied by its prime contractors.

Recommendation, Management Comments, and Audit Response

B. We recommend that the Director, Wright Laboratory, terminate the Cluster Tool Process Enhancement of the MMST contract.

Air Force Comments. The Deputy Assistant Secretary of the Air Force (Management Policy and Program Integration) nonconcurred with the finding and recommendation. The Air Force stated that MMST technology is very much needed for both DoD and commercial applications. The MMST Program provides low-cost manufacturing techniques for low-volume production of specialty parts. Personnel at NSA are aware that MMST technology would be beneficial in their applications and may consider using at least some of it in future upgrades to their facility. Extensive planning for the follow-on program included discussions of requirements with DoD organizations such as NSA, the Defense Nuclear Agency, Sandia National Laboratory, and Phillips Laboratory. Even though none of those organizations had plans to implement a full MMST-type facility, they expressed great interest in the technology and wanted it to be diffused throughout the semiconductor industry so that the technology could be available to DoD.

The Air Force indicated that the focus of the MMST Program was not to provide facilities for DoD, but to demonstrate concepts for the low-cost, flexible manufacture of ASICs in low volume. The Air Force indicated that DoD requirements for ASIC production facilities are irrelevant in determining the need for MMST technology. The benefits of the MMST Program and resulting technology can be realized by procuring integrated circuits from other facilities, either directly or through contractors, that utilize MMST technology in whole or in part. Furthermore, aspects of MMST technology can be incorporated into existing facilities without the purchase of an entire MMST factory. The MMST Program intends to demonstrate concepts for cost-effective, flexible manufacturing throughout the semiconductor industry.

Regarding the recommendation, the Air Force stated that many low-cost, flexible manufacturing techniques were unheard of before the MMST Program was implemented. Those manufacturing techniques are now commonly used by the semiconductor industry and are starting to be used in other device processing industries. The follow-on Cluster Tool Process Enhancement task is intended to extend those manufacturing techniques to include improved dry clean-up processes and flexible production of silicon-on-insulator devices.

All of those techniques are aimed at affordability in processing low-volume, specialty devices for DoD. The full text of the Air Force comments is in Part IV.

Audit Response. We agree with the Air Force comments regarding the MMST Program's success in demonstrating the feasibility of developing low-cost manufacturing techniques for ASICs. However, as indicated in the finding, we found no evidence to justify continuation of the MMST Program. Despite the Air Force comments, our discussions with managers at the organizations referenced by the Air Force (NSA, the Defense Nuclear Agency, Sandia National Laboratory, and Phillips Laboratory) indicated that they had little interest in continuation of the Program. None of the organizations we contacted had plans to integrate MMST applications into their operations.

Further, we disagree that the MMST Program contribution to the U.S. semiconductor industry warrants its continuation. We identified no specific shortfall within DoD regarding the availability of ASICs from commercial sources. Accordingly, we believe that no further expenditures of Air Force funds to develop the MMST based on an intrinsic and somewhat nebulous contribution to the DoD and the U.S. semiconductor industry are warranted. If such an effort is needed, it would be more appropriately funded by the Advanced Research Projects Agency, which has the specific mission of developing the U. S. industrial base to include the semiconductor industry. We request that the Air Force reconsider its position in response to this final report.

Part III - Additional Information

Appendix A. Glossary

Application Specific Integrated Circuit. Circuits designed for a specific purpose and usually produced in low volumes.

Chip. A single square or rectangular piece of semiconductor material into which a specific electrical circuit has been fabricated.

Clean Room. A room in which air quality is maintained and controlled by a filtering system that is sensitive to dirt particles in the air. A class 1 clean room has less than one .5 micron dirt particle per cubic foot of air. A class 10 clean room has less than 10 dirt particles of .5 micron or larger per cubic foot of air. A class 100 clean room has less than 100 dirt particles of .5 micron or larger per cubic foot of air.

Class B Chip. A microelectronics chip that must pass stringent stress and environmental tests to meet a specified reliability standard for all applications except outer space applications.

Complementary Metal Oxide Semiconductor. The design and fabrication of devices by interconnecting both positive and negative metal oxide semiconductor transistors.

Gallium Arsenide. A synthetic compound used especially as a semiconducting material.

Gate Array. Digital logic on a single die matrix with transistors not connected or interacting; may be in multiple layers.

Indium Phosphide. A malleable, fusible, silvery, metallic element, that is used in making transistors.

Integrated Circuit. An electronic circuit made by fabricating components such as resistors, capacitors, and transistors on a single piece of semiconductor material, usually silicon. A semiconductor chip containing multiple elements that act together to form the complete device circuit.

Mask. A flat, transparent glass plate that contains the image of circuit patterns to be placed on one layer of a wafer during the manufacture of an integrated circuit.

Maskmaking. The process whereby each layer of a circuit design is photographically transposed onto a glass plate.

Micron. One millionth of a meter.

Scribed. To mark a line by etching or cutting with a pointed instrument.

Silicon on Sapphire. A metal oxide semiconductor technology in which silicon is grown where needed on a sapphire wafer. Each circuit is thus isolated by air or oxide from other circuits.

Wafer. A thin disk of semiconducting material (usually silicon) on which many separate chips can be fabricated and then cut into individual integrated circuits.

Appendix B. Executive Summary of Audit Report No. 94-195

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Office of the Inspector General, DoD

Report No. 94-195 September 23, 1994
(Project No. 3RC-0026.01)

PAY DIFFERENTIALS AT THE NATIONAL SECURITY AGENCY'S MICROELECTRONIC FACILITIES

EXECUTIVE SUMMARY

Introduction. The National Security Agency (the Agency) operates a microelectronic chip manufacturing facility, the Special Processing Laboratory. Also, Agency personnel assemble printed circuit boards in the Special Processing Laboratory building. The Agency performs research on microelectronic chip design and semiconductor processing at its Microelectronic Research Laboratory. Toxic chemicals and gases are used at the Special Processing Laboratory and the Microelectronic Research Laboratory. The Agency authorized the payment of hazard and environmental pay differentials for the NSA (b)(3) employees who work in both laboratories.

Objective. The audit objective was to evaluate the propriety of paying hazard and environmental pay differentials to Agency personnel who work with or in close proximity to toxic chemicals or with the risk of chemical leakage or spillage.

Audit Results. The Agency did not place sufficient emphasis on engineering and administrative controls that had reduced hazardous and unsafe conditions to a negligible level in determining whether to authorize hazard and environmental pay differentials Consequently, the Agency is making unnecessary payments for hazard and environmental pay differentials for work in the Special Processing Laboratory and the Microelectronic Research Laboratory

Internal Controls. The audit did not identify material internal control weaknesses See Part I of this report for the internal controls assessed.

Potential Benefits of Audit. By terminating unneeded hazard and environmental pay differentials, the Agency will be able to put NSA (b)(3) 50 USC 3605 to better use annually and NSA (b)(3) 50 USC 3605 to better use during the FY 1995 through FY 2000 Future Years Defense Program (see Appendix B).

Summary of Recommendations. We recommended that the Agency modify its Personnel Management Manual to authorize payments for hazard and environmental pay differentials for work only in those areas designated as potential health hazards by the Occupational Safety and Health Services Division and to cease paying hazard and environmental pay differentials for work performed in areas designated low-risk.

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Management Comments. The Director, National Security Agency, agreed to the recommended actions and indicated that the monetary benefits of NSA (b)(3) 50 USC 3605 will be achieved. The response also included comments on the working conditions in the Special Processing Laboratory and on factors affecting managers' decisions on determining whether pay differentials should be authorized. A discussion of the Director's response is in Part II, and the complete text of the comments is in Part IV.

Appendix C. Executive Summary Audit Report No. 95-008

UNCLASSIFIED

Office of the Inspector General, DoD

Report No. 95-008 October 12, 1994
(Project No 3RC-0026 02)

MICROELECTRONIC MANUFACTURING SCIENCE AND TECHNOLOGY PROGRAM (U)

EXECUTIVE SUMMARY (U)

(U) **Introduction.** This report resulted from the audit of DoD's Microelectronic Chip Manufacturing capabilities (Project No 3RC-0026.00) This segment of the audit reviewed the controls over technology developed under the Advanced Research Projects Agency's Microelectronic Manufacturing Science and Technology (MMST) program The objective of the MMST program was to demonstrate concepts for the flexible, cost-effective, low-volume manufacture of application-specific integrated circuits The Advanced Research Projects Agency, the Air Force, and Texas Instruments, Incorporated (Texas Instruments) expended about $86.0 million on the MMST program.

(U) **Objective.** The audit objective was to determine whether sufficient policies, procedures, and internal controls have been established to safeguard technology developed under the MMST program.

(U) **Audit Results.** Wright Laboratory, Wright-Patterson Air Force Base, Department of the Air Force, did not effectively safeguard technology developed under the MMST program As a result, Texas Instruments inappropriately licensed MMST technology to a foreign company.

(U) **Internal Controls.** The audit identified no material internal control weaknesses However, Wright Laboratory later modified the internal controls established in the MMST contract clauses that safeguarded the technology developed under the MMST program See Part I of this report for the internal controls assessed.

(U) **Potential Benefits of Audit.** This report identifies no monetary benefits Nonmonetary benefits include improved controls over the transfer of the MMST technology and compliance with applicable laws and regulations

(U) **Summary of Recommendations.** We recommended that the Director, Wright Laboratory, notify Texas Instruments to obtain the appropriate licenses required by the International Traffic in Arms Regulation and the Export Administration Regulation before selling or licensing MMST technology to foreign governments or companies We also recommended that the Director provide Texas Instruments a more definitive description of what constitutes a suitable vendor for commercializing MMST technology

(U) **Management Comments.** The Air Force did not provide comments on a draft of this report We request comments from the Director, Wright Laboratory, by November 14, 1994

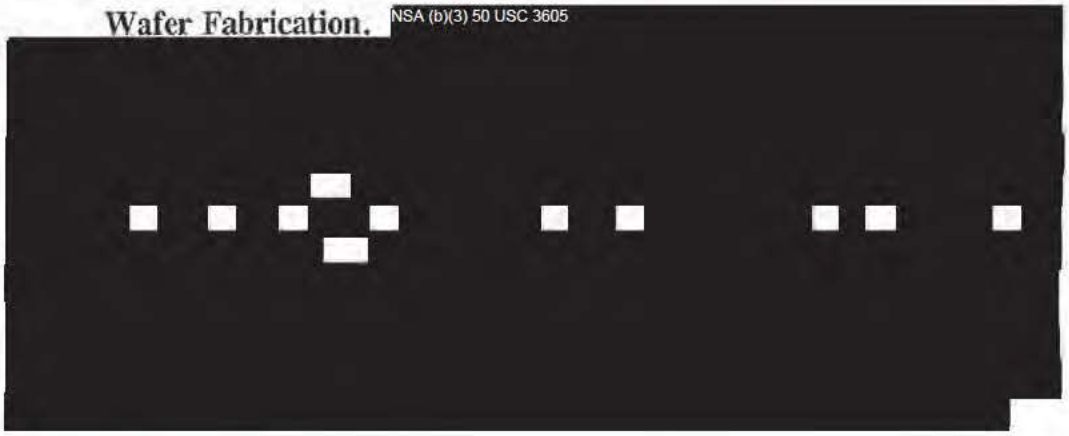
UNCLASSIFIED

Appendix D. Special Processing Laboratory Operations

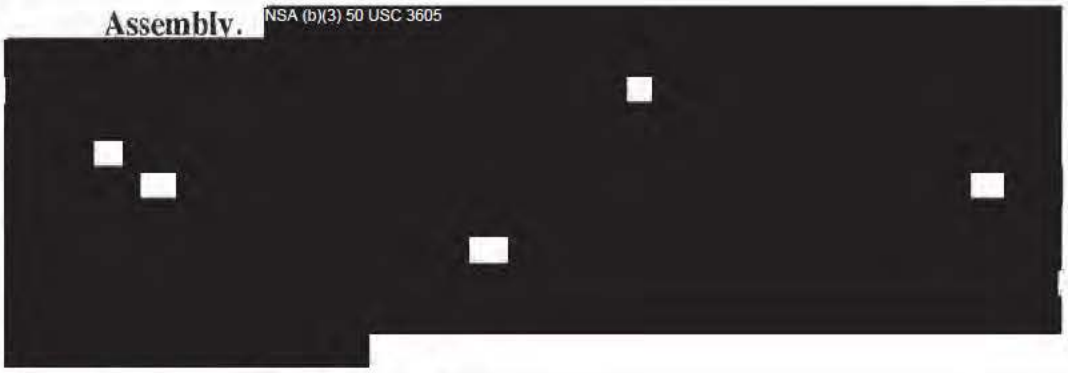
The microelectronics chip manufacturing process at the SPL is performed in four major functional areas: maskmaking, wafer fabrication, assembly, and testing.

Maskmaking. NSA (b)(3) 50 USC 3605

Wafer Fabrication. NSA (b)(3) 50 USC 3605



Assembly. NSA (b)(3) 50 USC 3605



Testing. NSA (b)(3) 50 USC 3605

Appendix D. Special Processing Laboratory Operations

NSA (b)(3) 50 USC 3605

[redacted]

Appendix E. DoD Microelectronics Chip Manufacturing Capabilities

Department of the Army Capabilities

Army Research Laboratory, Electronic Technology and Devices Directorate, Fort Monmouth, New Jersey. The Army Research Laboratory, Fort Monmouth, New Jersey, conducts research on electronic devices used within military systems. The Laboratory annually produces about 100 ASICs for a variety of research projects on gallium arsenide wafers in a class 10 clean room environment.

Army Research Laboratory, High Power Microwave Technology Directorate, Adelphi, Maryland. The Army Research Laboratory, Adelphi, Maryland, formulates, develops, and manages a comprehensive technology research program and performs analysis experimentation and concept demonstration to support Army and DoD requirements. The laboratory conducts research in the radiation hardening of chips, but does not have ASIC chip manufacturing capabilities.

Department of the Navy Capabilities

Naval Research Laboratory, Electronics Science and Technology Division, Washington, D.C. The Naval Research Laboratory, Washington, D.C., conducts research and development in microelectronics for new Navy applications. The laboratory is capable of fabricating a limited number of 3.5 micron prototype ASICs using gallium arsenide or a complementary metal oxide semiconductor on a silicon wafer. The Naval Research Laboratory has a class 100 clean room.

Naval Command and Control Ocean Surveillance Center; Microelectronics Laboratory; Research, Development, Test, and Evaluation Division, San Diego, California. The Naval Command and Control Ocean Surveillance Center, San Diego, California, is the Navy's principal facility for process research, design analysis, and field production of silicon integrated circuits for military applications. The Center is the only full-service silicon design, fabrication, test, and packaging facility among the Military Departments. The center is capable of producing approximately 1,500 wafers annually using an ultrathinfilm, silicon-on-sapphire technology and an indium phosphide materials and alloys technology. The Center does not manufacture ASICs.

Department of the Air Force Capabilities

Sacramento Air Logistics Center, McClellen Air Force Base, Sacramento, California. The Sacramento ALC applies state-of-the-art microelectronics technology to military systems to achieve improvements in performance, reliability, and maintainability. The center buys generic chips on 6-inch wafers and either fine tunes the chips or produces prototype circuit boards to satisfy customer requirements. The center specializes in modernizing obsolete parts that the Air Force is still using in operational systems. The center does not have chip manufacturing capabilities.

Ogden Air Logistics Center, Hill Air Force Base, Ogden, Utah. The Ogden ALC has test and design capabilities for field programmable gate arrays. The Center utilizes those capabilities to enhance the performance of existing Air Force systems. The center does not have chip manufacturing capabilities.

Phillips Laboratory, Hanscom Air Force Base, Lincoln, Maine. Phillips Laboratory, Hanscom Air Force Base, performs research in radiation hardening technology for use in Air Force and DoD space environments. Phillips laboratory does not have chip manufacturing capabilities.

Phillips Laboratory, Kirtland Air Force Base, Albuquerque, New Mexico. Phillips Laboratory, Kirtland Air Force Base, conducts research and development on the latest technologies relating to high-altitude electronic systems, radiation hardened chips, and space qualified integrated circuits. The laboratory does not have chip manufacturing capabilities.

Rome Laboratory, Hanscom Air Force Base, Lincoln, Maine. Rome Laboratory, Hanscom Air Force Base, conducts research and development in the solid-state sciences, reliability sciences, and electromagnetic areas. Rome Laboratory designs chips for use in current or future systems, but does not have chip manufacturing capabilities.

Wright Laboratory, Solid State Electronics Directorate, Wright-Patterson Air Force Base, Dayton, Ohio. Wright Laboratory, Wright-Patterson Air Force Base, directs and conducts contractual and in-house research to develop a technology base for advanced solid-state electronics. Wright Laboratory has a class 100 clean room and produces prototype chips using a .10-micron-level gallium arsenide process.

Federally Funded Research and Development Center Capabilities

Lincoln Laboratory, Massachusetts Institute of Technology, Hanscom Air Force Base, Lincoln, Maine. Lincoln Laboratory, Hanscom Air Force Base, develops and delivers specialized microelectronics circuitry components to Government agencies.

Lincoln Laboratory conducts research programs to advance the state-of-the-art in microelectronics devices and fabrication technology with special emphasis on dual use technology. The laboratory fabricates 1,000 chips annually on silicon and occasionally on thin film gallium arsenide.

Appendix F. Summary of Potential Benefits Resulting From Audit

Recommendation Reference	Description of Benefit	Amount and/or Type of Benefit
1.	Economy and Efficiency. Implementation should result in greater utilization of the SPL.	Undeterminable. The value of commercial purchases of unclassified ASICs that could be manufactured at the SPL cannot be determined.
2.	Economy and Efficiency. Implementation should avoid expenditures for continued development of the MMST program.	$7.4 million (see Note below) in Research, Development, Test and Evaluation funds put to better use for FY 1995 through FY 1998.

Note. Funds put to better use by fiscal year ($ in millions).

Type of Funds	Program Element	1995	1996	1997	1998	Total
RDT&E*	70811F	$0.9	$2.7	$3.4	$.04	$7.4

*Research, Development, Test, and Evaluation

Appendix G. Organizations Visited or Contacted

Office of the Secretary of Defense

Under Secretary of Defense for Acquisition and Technology, Washington, DC
Director, Defense Research and Engineering, Washington, DC
Assistant Secretary of Defense (Command, Control, Communications and Intelligence), Washington, DC
Assistant Secretary of Defense (Economic Security), Washington, DC

Department of the Army

Army Depot Systems Command, Tobyhanna Army Depot, PA
Sacramento Army Depot, Sacramento, CA
Army Materiel Command, Alexandria, VA
Army Research Laboratory, Adelphi, MD
Electronics Technology and Devices Division, Fort Monmouth, NJ
Army Missile Command, Redstone Arsenal, AL
Army Strategic Defense Command, Huntsville, AL
Directorate of Information Management, Army Communications-Electronics Command, Fort Monmouth, NJ
Directorate of Information Management, 1st Infantry Division (Mechanized), Fort Riley, KS
Instrumentation Development Directorate, White Sands Missile Range, NM

Department of the Navy

Office of Naval Research, Washington, DC
Electronics Science and Technology Division, Naval Research Laboratory, Washington, DC
Naval Command and Control Ocean Surveillance Center, San Diego, CA
Navy Public Works Center, San Diego, CA
Naval Regional Contracting Center, Long Beach, CA
Naval Supply Center, Puget Sound, WA
Naval Surface Warfare Center, Crane, IN
Naval Contracting Center, San Diego, CA
Aircraft Division, Naval Air Warfare Center, Indianapolis, IN
Weapons Division, Naval Air Warfare Center, China Lake, CA

Department of the Air Force

Air Force Command, Control, Communications, and Computer Agency, Scott Air Force Base, IL
Ogden Air Logistics Center, Hill Air Force Base, UT
Sacramento Air Logistics Center, McClellan Air Force Base, CA
Oklahoma City Air Logistics Center, Tinker Air Force Base, OK
Warner-Robins Air Logistics Center, Robins Air Force Base, GA
Space and Space Missile Systems Center, Los Angeles, CA
Electronic Systems Center, Hanscom Air Force Base, MA
Communications Systems Center, Tinker Air Force Base, OK
Phillips Laboratory, Hanscom Air Force Base, MA
Phillips Laboratory, Kirtland Air Force Base, NM
Rome Laboratory, Hanscom Air Force Base, MA
Wright Laboratory, Wright-Patterson Air Force Base, OH
384th Comptroller Squadron (now 22nd Comptroller Squadron), McConnell Air Force Base, KS
544th Range Squadron, Nellis Air Force Base, NV

Defense Agencies

Advanced Research Projects Agency, Arlington, VA
Central Imagery Office, Arlington, VA
Defense Logistics Agency, Alexandria, VA
Defense Electronics Supply Center, Dayton, OH
National Security Agency, Fort Meade, MD
National Reconnaissance Office, Washington, DC

Non-DoD Organizations

Department of Energy, Sandia National Laboratories, Albuquerque, NM

Non-Government Organizations

Massachusetts Institute of Technology, Lincoln Laboratory, Hanscom Air Force Base, MA
Semiconductor Manufacturing Technology Consortium, Incorporated, Austin, TX
Texas Instruments, Incorporated, Dallas, TX

Appendix H. Report Distribution

Office of the Secretary of Defense

Under Secretary of Defense for Acquisition and Technology
Under Secretary of Defense (Comptroller)
Under Secretary of Defense (Comptroller), Deputy Comptroller (Program/Budget)
Director, Defense Research and Engineering
Assistant Secretary of Defense (Command, Control, Communications and Intelligence)

Department of the Army

Auditor General, Department of the Army

Department of the Navy

Auditor General, Department of the Navy

Department of the Air Force

Secretary of the Air Force
Assistant Secretary of the Air Force (Financial Management and Comptroller)
Deputy Assistant Secretary of the Air Force (Management Policy and Program Integration)
Auditor General, Department of the Air Force

Defense Organizations

Director, Advanced Research Projects Agency
Director, Defense Contract Audit Agency
Director, Defense Logistics Agency
Director, National Security Agency
Inspector General, Central Imagery Office
Inspector General, National Security Agency

Non-Defense Federal Organizations

Office of Management and Budget
National Security and International Affairs Division, Technical Information Center, General Accounting Office

Chairman and Ranking Minority Member of Each of the Following Congressional Committees and Subcommittees:

Senate Committee on Appropriations
Senate Subcommittee on Defense, Committee on Appropriations
Senate Committee on Armed Services
Senate Committee on Governmental Affairs
Senate Select Committee on Intelligence
House Committee on Appropriations
House Subcommittee on Defense, Committee on Appropriations
House Committee on Government Reform and Oversight
House Subcommittee on National Security, International Affairs, and Criminal Justice, Committee on Government Reform and Oversight
House Committee on National Security
House Permanent Select Committee on Intelligence

Part IV - Management Comments

Department of the Air Force Comments

DEPARTMENT OF THE AIR FORCE
WASHINGTON DC

25 JAN 1995

OFFICE OF THE ASSISTANT SECRETARY

MEMORANDUM FOR ASSISTANT INSPECTOR GENERAL FOR AUDITING
OFFICE OF THE INSPECTOR GENERAL
DEPARTMENT OF DEFENSE

FROM: SAF/AQX
1060 Air Force Pentagon
Washington DC 20330-1060

SUBJECT: DoD IG Draft Audit Report on Microelectronics Chip Manufacturing, Nov 23, 1994 (Project No. 3RC-0026)

This is in reply to your request for Air Force comments on the subject report.

We have reviewed the subject draft report and do not concur in several of the findings, as detailed in the attached comments. In addition, we do not concur in the recommendation of Finding B concerning the Microelectronics Manufacturing Science and Technology (MMST) program.

Our point of contact is DoD OIG (b)(6), SAF/AQXM, DSN DoD OIG (b)(6) or DoD OIG (b)(6).

BLAISE J. DURANTE
Deputy Assistant Secretary
(Management Policy & Program Integration)
Assistant Secretary (Acquisition)

Attachment:
Air Force Comments

Air Force Comments
on
DoD IG Draft Audit Report
on
Microelectronics Chip Manufacturing
Nov 23, 1994
(Project No. 3RC-0026)

1. **Page ii, Summary of Recommendations:** "We recommend that the Director, National Security Agency, increase the utilization of the Special Processing Laboratory by manufacturing unclassified microelectronics chips at the Special Processing Laboratory NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) [redacted]."

Air Force comment: We do not advocate such a generalized recommendation for all unclassified microelectronics chips since it is often much more cost-effective to procure them from a facility that is tailored to the volumes and technologies required. An advantage in economy of scale can often be realized from commercial sources since labor and overhead costs can be amortized across a larger number of orders. We note that the recommendation on page 14 is more reasonable: "We recommend that the Director, National Security Agency...determine whether the Special Processing Laboratory can produce unclassified microelectronics chips NSA (b)(3) 50 USC [redacted] NSA (b)(3) 50 USC 3605 and 50 USC 3024(i) [redacted] We nonconcur in the recommendation on page ii, but concur in the recommendation on page 14.

2. **Page 2, Microelectronic Chip Manufacturing Facilities:** "...facilities cost about $175 million to build..."

Air Force comment: The current costs of some state-of-the-art fabrication facilities are approaching $1 billion.

3. **Page 15, Finding B:** "Microelectronic Manufacturing Science Technology Program Completion."

Air Force comment: The correct title of the referenced program is "Microelectronics Manufacturing Science and Technology".

4. **Page 15, Finding B:** "The Air Force is planning an unneeded modification to the MMST contract, although DoD organizations have not demonstrated a need for the MMST technology already developed."

Air Force comment: We do not concur in this statement. MMST technology is very much needed for both DoD and commercial applications. Outstanding examples of this are the issues presented in Finding A of subject audit. MMST provides low cost manufacturing techniques that allow tailoring to required capacity and flexible processing for low volumes. These are the very problems cited in the audit report. Personnel at the National Security Agency

Department of the Air Force Comments

(NSA) are aware that MMST technology would be beneficial in their application, and may consider using at least some of it in future upgrades of their facility.

5. **Page 15, Finding B:** "...the program office did not verify whether the requirement was still valid."

Air Force comment: We do not concur in this statement. Extensive planning for the follow-on program included discussions of requirements with DoD organizations such as NSA, the Defense Nuclear Agency, Sandia National Laboratory, and Phillips Laboratory. Even though none of these organizations had plans to implement a full MMST-type facility, they expressed great interest in the technology and wanted it to be diffused throughout the semiconductor industry such that it could be available to DoD. This was concurrent with the objective of the program.

6. **Page 15, Goals and Objectives:** "The MMST program focused on DoD's need for a low volume, ASIC production facility."

Air Force comment: We do not concur in this statement. The focus of the program was to demonstrate concepts for low cost, flexible manufacture of Application Specific Integrated Circuits (ASICs) in low volume. The objective was not to provide facilities for DoD.

7. **Page 15, Cost Sharing and Project Modification:** "Texas Instruments...agreed to absorb 32 percent of the MMST program's development cost."

Air Force comment: We concur in this statement and add that Texas Instruments was very willing to cost share the program so that they could maintain many of the data rights.

8. **Page 15, Cost Sharing and Project Modification:** "In May 1991, Wright Laboratory modified the contract requirements and reduced the value to $86 million."

Air Force comment: We concur in this statement and add the following information. This downscope was a bilateral agreement. It was based on the fact that budgets were limited. The downscoped contract emphasized the demonstration of concepts and removed requirements to build a facility.

9. **Page 16, Cost Sharing and Project Modification:** "The Wright Laboratory project managers did not determine whether the organizations identified in 1988 were still interested in the MMST program when the managers initiated the modification."

Air Force comment: We do not concur in this statement. The project managers did determine that there was still great interest in MMST before initiating the follow-on program. See paragraph 5 above.

10. Page 16, MMST Accomplishments: "The MMST program has been recognized as a significant accomplishment in enhancing the design and engineering of small volume integrated circuit manufacturing capabilities."

Air Force comment: This statement reads more accurately by deleting the words "the design and engineering of".

11. Pages 16-17, DoD Requirement for MMST Facilities, all paragraphs.

Air Force comment: We maintain that facility requirements in DoD are irrelevant in determining the need for MMST technology. The benefits of this program and resulting technology can be realized by procuring integrated circuits from other facilities, either directly or through contractors, which utilize MMST technology in whole or part. Furthermore, aspects of MMST technology can be incorporated into existing facilities without purchasing an entire MMST factory. The program intends to demonstrate concepts for cost-effective, flexible manufacturing and migrate them throughout the industry, not provide facilities for DoD.

12. Page 16, MMST Procurements: "Although MMST technology is providing a technical base for use by microelectronics equipment manufacturers, none of the DoD organizations identified by the MMST program office in 1988 are planning to procure MMST facilities."

Air Force comment: Procurement of facilities by these organizations was not the emphasis of MMST and is irrelevant in determining the need for MMST technology.

13. Page 16, Sacramento-ALC Requirements: "...the MMST program office had not identified the annual cost of operating an MMST facility," and page 17, same paragraph, "...a fully operational MMST facility could produce 50,000 chips annually."

Air Force comment: We concur in these statements but add the following information. The operating cost and production level of an MMST facility are highly dependent on a number of factors, including existing infrastructure, chip complexity, and configuration of the facility. Facilities using MMST technology are modular and can be tailored to required production levels.

14. Page 17, Ogden-ALC Requirements: "...personnel determined that a different type of chip, the Field Programmable Gate Array, provided a more cost-effective alternative."

Air Force comment: We neither concur nor nonconcur in this statement but question how long this gate array technology will meet requirements that are ever-increasing in complexity.

15. Page 17, National Security Agency Requirements: "...since the SPL is following the lead of the National Semiconductor Corporation in obtaining manufacturing technology, SPL personnel did not further consider procuring an MMST facility."

Air Force comment: We neither concur nor nonconcur in this statement but offer the following information. National Semiconductor Corporation has attended most, if not all, MMST Industry Reviews and has been interested in incorporating MMST concepts into their facilities. Also, personnel from the Microelectronics Research Laboratory (MRL) at NSA attended MMST reviews, as well as meetings for the follow-on program, and continue to have an interest in this technology.

16. Page 17, Other DoD Component Requirements: "No other DoD Component had requirements for the MMST program."

Air Force comment: We do not concur in this statement because we do not understand how this conclusion is reached. Any organization that buys low volume devices, directly or indirectly, can potentially benefit from MMST technology, whether or not they purchase a facility. If DoD components wish to reduce costs for electronic systems, then it does not make sense that they have no requirements for MMST technology.

17. Page 17, Microelectronics Chip Requirements: "DoD organizations were not purchasing ASICs directly from chip manufacturers" and "DoD organizations were procuring circuit boards with the chips attached."

Air Force comment: We concur in these statements and add the following. Because devices are typically bought by DoD through contractors, it is important that MMST technology be diffused throughout the industry to enhance manufacturing flexibility and lower the cost of low volume, specialty parts. This emphasizes the fact that technology transfer and commercialization are very important in the MMST program--more important than providing facilities for DoD organizations.

18. Page 18, Radiation Hardened Chips: "No DoD organization demonstrated a requirement for a capability to produce small quantities of radiation hardened chips."

Air Force comment: We neither concur nor nonconcur in this statement but emphasize that some of these organizations do need small quantities of radiation hard chips, whether or not they need the "capability to produce" them.

19. Page 18, Radiation Hardened Chips: "Their primary contractors were providing them the needed chips."

Air Force comment: We concur in this statement and add the following. For this reason, MMST technology must be developed and transferred. The cost savings from flexible production of small quantities of radiation hard chips by contractors can be passed on to DoD organizations.

20. Page 18, Radiation Hardened Chips: "...the Department of Energy has the capability to produce limited quantities of radiation hardened chips at its Sandia Laboratory."

Air Force comment: We concur in this statement and add that the Sandia Laboratory can potentially improve its current operation by increasing flexibility, reducing cycle times, and reducing capital costs with MMST technology.

21. **Page 18, Radiation Hardened Chips:** "...the Consortium [SEMATECH] had initiated research into the production of silicon-on-insulator chips that could meet requirements for radiation hardened chips."

Air Force comment: We neither concur nor nonconcur in this statement but add that SEMATECH's primary focus has typically been high volume manufacturing. Also, much technology already exists for processing silicon-on-insulator devices; MMST is demonstrating how to process them in low volumes more efficiently, i.e., at lower cost.

22. **Page 18, Radiation Hardened Chips:** "Consequently, there is no requirement to continue the silicon-on-insulator process flow continuation to the MMST program."

Air Force comment: We do not concur in this statement. The facts stated in the above comments serve to significantly weaken the argument that supports this conclusion.

23. **Page 18, Modification Status as of October 30, 1994:** "That action [stop work order] took place before Texas Instruments initiated work on the modification."

Air Force comment: This statement is incorrect because Texas Instruments had accomplished work in the dry clean-up area before the stop work order was issued.

24. **Page 18, Program Continuation:** "Continuation of the MMST program is not warranted."

Air Force comment: We do not concur in this statement for the reasons stated in the above comments related to Finding B.

25. **Page 18, Program Continuation:** "...other than NSA, no DoD organization has demonstrated a requirement for the MMST program."

Air Force comment: We do not concur in this statement. Any organization that has a need for small quantities of specialty devices can benefit from MMST technology, and all DoD organizations have a requirement for reduced costs.

26. **Page 18, Program Continuation:** "Since NSA already has a facility that is underutilized, the development of additional capabilities is unneeded."

Air Force comment: We do not concur in this statement. NSA could cost-effectively tailor the capacity of their facility using MMST technology. If additional capabilities will improve production and reduce costs, then their development is most certainly needed. MMST technology is intended to do just that.

Department of the Air Force Comments

27. Page 19, Program Continuation: "...DoD's requirement for radiation hardened chips is being sufficiently satisfied by its prime contractors."

Air Force comment: We neither concur nor nonconcur in this statement but add that cost savings can be realized by DoD through prime contractors by diffusing MMST technology throughout industry.

28. Page 19, Recommendation For Corrective Action: "We recommend that the Director, Wright Laboratory, terminate the Cluster Tool Process Enhancement of the MMST contract."

Air Force comment: We do not concur in this recommendation. The findings in this report are not strong enough to support the recommended termination. There are many good reasons for continuing this program, many of which have been stated in the above comments. Also, there are no findings that specifically pertain to the dry clean-up processes, which constitute nearly the same amount of effort (25%) as silicon-on-insulator processing (28%) in the Cluster Tool Process Enhancement task.

We do not concur in the recommendation to terminate the MMST follow-on and request that this recommendation be reconsidered by the DoD IG. MMST has demonstrated low cost, flexible manufacturing techniques such as single-wafer processing, modular (cluster tool) equipment, in situ sensors, real time process control, and an object oriented, distributed computer integrated manufacturing system. Many of these techniques, which were unheard-of prior to the MMST program, are now in common use by the semiconductor industry and are migrating to other device processing industries, such as focal plane array and flat panel display manufacturing. The follow-on Cluster Tool Process Enhancement task is intended to extend these techniques to include improved dry clean-up processes and flexible production of silicon-on-insulator devices All of these techniques are aimed at affordability in processing low volume specialty devices for DoD.

National Security Agency Comments

NATIONAL SECURITY AGENCY
FORT GEORGE G. MEADE, MARYLAND 20755-6000

Serial: COMP-003-95
24 January 1995

MEMORANDUM FOR THE DIRECTOR, READINESS AND OPERATIONAL SUPPORT DIRECTORATE, DOD OIG

SUBJECT: Draft Audit Report on Microelectronics Chip Manufacturing (Project No. 3RC-0026) – INFORMATION MEMORANDUM

1. The subject audit report, dated 23 November 1994, has been reviewed, and the following information is provided.

NSA (b)(3) 50 USC 3605 and 50 USC 3024(i)

[redacted]

b. Before NSA can concur or nonconcur with the recommendation for Finding A , a review will be conducted of pertinent Agency acquisition policy. A position will be available by 25 May 1995.

2. Please contact NSA (b)(3) 50 USC 3605 [redacted], if you have any questions or need additional information.

NSA (b)(6) [redacted]

J. STEPHEN TURETT
COMPTROLLER

Audit Team Members

This report was prepared by the Readiness and Operational Support Directorate, Office of the Assistant Inspector General for Auditing, Department of Defense.