Defense Microelectronics Activity (DMEA)
2024.1 Small Business Innovation Research (SBIR)
Proposal Submission Instructions

INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR/STTR Program is implemented, administrated, and managed by the DMEA Office of Small Business Programs (OSBP). Proposers responding to a topic in this BAA must follow all general instructions provided in the Department of Defense (DoD) SBIR Program BAA. DMEA requirements in addition to or deviating from the DoD Program BAA are provided in the instructions below.

Proposers are encouraged to thoroughly review the DoD Program BAA and register for the DSIP Listserv to remain apprised of important programmatic and contractual changes.

- The DoD Program BAA is located at: https://www.defensesbirsttr.mil/SBIR-STTR/Opportunities/#announcements. Be sure to select the tab for the appropriate BAA cycle.
- Register for the DSIP Listserv at: https://www.dodsbirsttr.mil/submissions/login.

Specific questions pertaining to the administration of the DMEA SBIR/STTR Program, and these proposal preparation instructions should be directed to the DMEA Acting SBIR/STTR Program Manager (PM), Mr. Tien Dang, at osd.mcclellan-park.dmea.list.smbus@mail.mil.

PHASE I PROPOSAL GUIDELINES

The Defense SBIR/STTR Innovation Portal (DSIP) is the official portal for DoD SBIR/STTR proposal submission. Proposers are required to submit proposals via DSIP; proposals submitted by any other means will be disregarded. Detailed instructions regarding registration and proposal submission via DSIP are provided in the DoD SBIR Program BAA.

DMEA intends for Phase I to be only an examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding $197,283.00. The technical period of performance for the Phase I effort should be no more than six (6) months.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please ensure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PROPOSAL VOLUMES:

Proposal Cover Sheet (Volume 1)

Required per the DoD SBIR Program BAA.

Technical Volume (Volume 2)

The technical volume is not to exceed twenty (20) pages and must follow the formatting requirements provided in the DoD SBIR Program BAA. Technical volumes exceeding twenty (20) pages will be deemed non-compliant and will not be evaluated.

Content of the Technical Volume

Read the DoD SBIR Program BAA for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be accepted.

DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DoD SBIR Program BAA. Due to limited funding, DMEA reserves the right to limit awards under any topic, and only proposals considered to be of superior quality will be funded.

Cost Volume (Volume 3)

The Phase I Base amount must not exceed $197,283.00. DMEA will conduct a price analysis to determine whether cost proposals, including quantities and prices, are fair and reasonable. Contractors should expect that cost proposals will be negotiated. Costs must be separated and clearly identified on the Proposal Cover Sheet (Volume 1) and in Volume 3.

The on-line cost volume for Phase I and Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a. through h. below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a. through h. below) as an appendix in your technical proposal. The itemized cost volume information (a. through h. below) will not count against the page limit on Phase I and II proposal submissions.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting Officer, be advantageous to the Government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DoD Component; unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DoD Component.

b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.

c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include leased hardware, must provide an adequate lease versus purchase justification or rationale.

d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.

e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.

f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.

g. Subcontracts: Involvement of university or other consultants in the planning and/or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.

h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

Please review the updated Percentage of Work (POW) calculation details included in the DoD Program BAA. DMEA will not accept any deviation to the POW requirements.

Company Commercialization Report (CCR) (Volume 4)
Completion of the CCR as Volume 4 of the proposal submission in DSIP is required. Please refer to the DoD SBIR Program BAA for full details on this requirement. Information contained in the CCR will be considered by DMEA during proposal evaluations.

Supporting Documents (Volume 5)
All proposing small business concerns are REQUIRED to submit the following documents to Volume 5:

1. Contractor Certification Regarding Provision of Prohibition on Contracting for Certain Telecommunications and Video Surveillance Services or Equipment
2. Disclosures of Foreign Affiliations or Relationships to Foreign Countries
3. Disclosure of Funding Sources

Please refer to the DoD Program BAA for more information.

PHASE II PROPOSAL GUIDELINES
Phase II proposals may only be submitted by Phase I awardees. Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

The Technical Volume is not to exceed forty (40) pages and consists of a single PDF file with your firm name, topic number, and proposal number in the header of each page. All documentation should use no smaller than 10-point font on standard 8.5" X 11" paper with one-inch margins and not be in two-column format. Do not include blank pages.

Phase II proposals may be submitted for an amount not to exceed $1,315,219.00. The technical period of performance for the Phase II effort should be no more than twenty-four (24) months.

Phase I awardees may submit a Phase II proposal without invitation not later than sixty (60) calendar days

following the end of the Phase I contract. The Phase II proposal submission instructions are identified in the Phase I contract, Part I – The Schedule, Section H, Special Contract Requirements, "SBIR Phase II Proposal Submission Instructions".

All Phase II proposals must have a complete electronic submission per the Proposal Volumes area listed in Phase I. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be considered for award.

Due to limited funding, DMEA's ability to award any Phase II, regardless of proposal quality or merit, is subject to availability of funds. Please ensure that your proposal is valid for 120 days after submission. Any extension to that time period will be requested by the Contracting Officer.

A Phase II contractor may receive up to one additional, Sequential Phase II award for continued work on a project. The additional, Sequential Phase II award has the same guideline amounts and limits as an initial Phase II award. Sequential, Phase II proposals shall be initiated by the Government Technical Point of Contact for the initial Phase II effort and must be approved by the Acting DMEA SBIR/STTR Program Manager in advance.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM

To encourage transition of SBIR into DoD systems, DMEA has a Phase II Enhancement policy. DMEA's Phase II Enhancement program requirements include up to one-year extension of existing Phase II and up to $657,610.00 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

DISCRETIONARY TECHNICAL AND BUSINESS ASSISTANCE (TABA)

DMEA does not provide Discretionary Technical and Business Assistance (TABA).

EVALUATION AND SELECTION

All proposals will be evaluated in accordance with the evaluation criteria listed in the DoD SBIR Program BAA Proposing firms will be notified of selection or non-selection status for a Phase I award within 90 days of the closing date of the BAA.

Refer to the DoD SBIR Program BAA for procedures to protest the Announcement.
As further prescribed in FAR 33.106(b), FAR 52.233-3, Protests after Award should be submitted to:

DMEA Acting SBIR/STTR Program Manager (PM):

- Name: Mr. Tien Dang
- Email: osd.mcclellan-park.dmea.list.smbus@mail.mil

DMEA SBIR 24.1 Topic Index

DMEA241-001 TITLE: Robotic Leak Repair for Cyclotron Vacuum Systems

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics, Space Technology, Trusted AI and Autonomy, Nuclear

OBJECTIVE: Develop a robotic system for leak location and repair of high-vacuum systems in cyclotrons and similar particle accelerators.

DESCRIPTION: Particle accelerators such as cyclotrons form a crucial link in enabling microelectronics in hostile radiation environments. Few facilities are available for Heavy Ion Single Event Effect testing in particular, which causes a bottleneck in the fielding of space systems and other programs with radiation environment requirements. These facilities are aging and heavily tasked, leaving little time and few resources for invasive repairs. Impacts to availability from insufficient maintenance or downtime for extensive repairs threaten limited and inelastic supply of beam time at these facilities. A major contributor to maintenance issues is leaks in the high-vacuum systems of the accelerators. Leak locations are frequently buried underneath other sensitive assemblies and in tightly confined spaces, particularly in the Radio Frequency tank and acceleration region of the cyclotron. Finding the location of these leaks if often invasive to the sensitive system, time consuming, and unreliable. Once found, leaks are difficult to repair with lasting solutions due to the mentioned access difficulties. Radioactivity in the vacuum components due to accelerator operation further slows and complicates maintenance actions, while representing a hazard to personnel. An innovative solution is proposed in the development of a robotic system capable of locating and repairing leaks in the high-vacuum system with greater speed, accuracy, and durability than possible using current manual methods. Further benefits would include reduction in invasive maintenance to the sensitive facilities and reduction in radiation hazard to personnel. Feasible solutions would need to be able to operate in the radiation environment of the accelerator vacuum, navigate the small inner dimensions of the vacuum system, locate and image leaks in the predominately copper systems, weld or otherwise enact lasting repairs to the located leaks, and reliably self-extract from the vacuum system while leaving no debris and only trace gasses in the vacuum system. The vacuum system would not need to be evacuated during operation of the robotic system. Key parameters are prioritized as follows:

1. Number of 90 degree bends the solution can tolerate for extraction after loss of robotic power or control
2. Minimum diameter the solution can traverse
3. Distance the solution can traverse through evacuated piping
4. Efficacy of sensors for locating leaks. Minimum detectable leak flow rate, minimum leak length/width for detection, or similar metric.
5. Ability to flag or map location of leaks without damage to vacuum system
6. Ability to enact durable repairs on located leaks
7. Estimated Total Ionizing Dose (TID) radiation tolerance of any non-exchangeable microelectronics, cabling, and material components inserted into the accelerator vacuum system. Any TID tolerance over 15 krad(SiO2) may be stated as ‘over 15 krad(SiO2)’ or similar language.

PHASE I: Perform a feasibility study on a robotic system for leak location and repair of high-vacuum systems in cyclotrons and other particle accelerators. Blockage or damage to the accelerator vacuum system by the proposed solution would be unacceptable. Emphasis will be placed on ensuring full recovery of the robotic system from the accelerator vacuum system in case of loss of power or control. Overall goal is to maximize the percent by length of the accelerator vacuum system serviceable with leak location and, separately, repair; while remaining fully recoverable and without posing danger to the vacuum system. The Lawrence Berkeley National Laboratory (LBNL) 88-inch cyclotron will be used as the baseline case for evaluating success. The feasibility study shall:

1. Describe a system capable of traversing a portion the vacuum system of the LBNL 88-inch cyclotron
2. Describe recovery mechanism for the system under loss of robotic power or control
3. Describe mechanisms for leak location
4. Describe mechanisms for mapping or marking located leaks
5. Describe mechanisms for durable repair of located leaks
6. Analyze the described solution against the key parameters from the above description
7. Provide a report including all all generated files (e.g., CAD drawings) and a program plan for system development

PHASE II: Phase II will result in building, testing and delivering a fully functional prototype of the solution developed in phase I. Testing shall include trials on piping models with attention to the parameters described in the description above. The prototype shall demonstrate recovery under simulated power and control loss scenarios from mock piping models. The prototype shall demonstrate location of a simulated vacuum leak. The prototype shall demonstrate non-destructive marking or mapping of located leaks. The prototype shall demonstrate durable repair of simulated leaks. Only after trials and demonstrations on mock piping models may any test be conducted on accelerator vacuum systems. Demonstration on actual accelerator vacuum systems is the goal of phase II testing, however, any access to accelerator vacuum systems is entirely at the discretion of LBNL or other facility.

PHASE III DUAL USE APPLICATIONS: Particle accelerator use is dominated by medical applications and scientific applications which outnumber and outspend the immediate DoD interest of Single Event Effect testing for microelectronics. Such facilities have similar vacuum systems and face similar challenges with their maintenance that could offer a market for robotic systems or services. Solutions to this proposal are also applicable to a wide variety of high vacuum facilities in various industries including advanced spectroscopy and microscopy, epitaxy growth and deposition facilities such as in the semiconductor industry, and science facilities such as gravitation wave detectors.

REFERENCES:

1. J. Benitez et al., “88-Inch Cyclotron Upgrades for Improved 20 MeV/nucleon Cocktail Beam Delivery,” 2023 Single Event Effects Symposium & Military And Aerospace Programmable Logic Devices Combined Workshop, La Jolla, California, USA, 2023.
2. M. K. Covo et al., "88-Inch Cyclotron: The one-stop facility for electronics radiation testing," 2017 IEEE International Workshop on Metrology for AeroSpace (MetroAeroSpace), Padua, Italy, 2017, pp. 484-488, doi: 10.1109/MetroAeroSpace.2017.7999622.

KEYWORDS: Heavy Ion particle accelerators, cyclotron, Ultra-High Vacuum systems, Single Event Effects, Robotics, Leak repair

DMEA241-002 TITLE: Development of Versatile Wafer Probe System for High Power Devices

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: Develop wafer probe systems (WPSs) for high voltage (HV) devices, e.g. metal-oxide semiconductor field-effect transistors (MOSFETs), diodes, and insulated-gate bipolar transistors (IGBTs) of wide-band gap (WBG) semiconductors such as silicon carbide (SiC). The system must include a wafer chamber, probes, electronics, environmental controllers, safety systems, and software. The WPS must be able to handle high voltage up to 40 kV with a current of 10 A (500A pulsed) through a wafer chuck and probes and must offer a versatile environment, including a vacuum and a wide range of temperatures. In addition, the WPS should also have the capability to perform accurate and reliable measurements of various electrical parameters.

DESCRIPTION: WBG semiconductors such as SiC are the most promising materials to develop high-power devices used in a variety of industries, including automobiles, home appliances, power applications, as well as aerospace and defense [1]. As the power electronics market and needs are growing rapidly, more powerful devices allowing more voltage and current are being developed, and this effort has accompanied the evolution of WPS, including source-meter units (SMUs) [2]. For the HV wafer level tests using WPSs, the moisture around wafers must be suppressed by environmental control to protect devices and to avoid early breakdown due to arcing or a strong electric field. To safely operate at HV, Fluorinert liquid has been introduced [3]. However, the application of liquid for electrical testing limits the ability to incorporate optical and/or thermal testing. Commercial manual wafer probers for high-power devices are available to handle up to 20 kV in air or fluorinated bath [4]. A WPS for HV under vacuum is also available [5]. However, WPSs for > 20 kV under vacuum and a wide-range of temperature are not available because of limited technological maturity. The proposed topic seeks to integrate hardware and software to handle 40 kV/10 A DC (500A pulsed) in a vacuum and a wide range of temperature. The final product must include a vacuum chamber with 6”-8” chuck (including cooling and heating system), probes, vibration isolation table, electrical system, software, and safety system.

PHASE I: Conduct a feasibility study and investigate the existing technique of HV WPS. Deliver the proposed design, circuits, simulation results, and parts list of a HV WPS that will be used to build a Phase II prototype. Propose sample types for the breakdown testing at 40 kV. The design must assure a high voltage of 40 kV and a high current of 10 A DC (500A pulsed) to test various characteristics of vertical SiC MOSFETs and diodes. The wafer chuck must be able to handle the high voltage and current. The sample chamber must provide a vacuum environment to minimize arcing and for low-temperature operation. The optical window must transmit a wide range of wavelengths, from ultraviolet (UV) to infrared (IR) . The proposed specifications of WPSs are below:

- Chamber:
    - Chuck must handle 6" – 8” wafers and 40kV/10A (500A pulsed)
    - Semi-automatic or full-automatic system
- Chuck automatic motion covering whole wafer range
- Probes may be manual for the semi-automatic system

    - Wafer/chuck temperature: ~77K – ~700K
- Must be able to continuously tune wafer temperature from ~77K to ~700K
- Must have a heater assembly and liquid nitrogen cooling/transfer capability; proportional–integral–derivative controller (PID) temperature control
    - Vacuum tight chamber: mechanical and turbo pumps for ~1E-5 Torr
    - Optical window
- Transmission wavelength: ~0.2um – >2 um
- Must have a blanket option to block the window
    - Microscopy with charge-coupled device (CCD) or complementary metal–oxide–semiconductor (CMOS) sensor
- Probes
    - 3 (three) probes with 4 (four) vacuum feedthroughs; 1 (one) additional vacuum feedthrough (blanked)
    - Probe tips/connectors/cables capable of handling 0–40 kV/0–10 A DC (500A pulsed) or more and a temperature of ~77K – ~700K
- Vibration isolation table
- Electrical system
    - Power supply capable of 0–40 kV
- Consider reverse bias for diode breakdown testing
- Capable of characterizing 3rd quadrant
- Capable of measuring body current across wafers
    - Arcing monitor/detector
- Software
    - Labview control; measurement control with analytical and mathematical operations
    - In-situ data visualization/plotting; data saving
    - Capable of characterizing current and voltage properties in the 3rd quadrant of HV vertical devices
    - Capable of controlling equipment (power supply, source-meter units, vacuum, temperature)
- Safety system
    - Interlock; arc monitor; operator safety physical shielding/keep-out/encloser

PHASE II: Build, test, and deliver a fully functional HV WPS prototype based on the design developed in Phase I. The prototype WPS will undergo rigorous testing to ensure its functionality and safety. This includes conducting various experiments to evaluate its performance under different conditions and scenarios. The final report will provide comprehensive technical documentation, including detailed drawings, circuit diagrams, part lists, and specifications, to facilitate the manufacturing process and address any challenges that were encountered during development. Once completed, the fully functional prototype WPS will be delivered to DMEA for further evaluation and implementation. Consider Underwriters Laboratories (UL)/International Electrotechnical Commission (IEC) regulation at this stage for future commercialization. UL/IEC regulatory certification ensures that the advanced system meets the necessary safety standards and guidelines, which is vital for its successful commercialization.

PHASE III DUAL USE APPLICATIONS: There may be opportunities for further development of this system for use in a specific military or commercial application. The Phase II effort aims to improve the testing capability of HV devices, which have various military applications, such as high-power microwave (HPM) pulse generators, electronic safety and arm devices, ignition safety devices, and flight termination systems. This enhancement will pave the way for Phase III, where a new generation of HV WPSs will be constructed. This advanced system will enable the characterization and testing of 40 kV WBG devices at the wafer-level, benefiting both military and commercial industries in multiple areas.

REFERENCES:

1. Krishna Shenai, Future Prospects of Widebandgap (WBG) Semiconductor Power Switching, IEEE Trans. Elec. Dev. 62, 248 (2015)
2. Miguel Hinojosa, et al., Evaluation of high-voltage, high-power 4H-SiC insulated-gate bipolar transistors, 2014 IPMHVC
3. Anant K. Agarwal, et al., 1.1 kV 4H-SiC power UMOSFETs, IEEE Elec. Dev. Lett. 18, 586 (1997)
4. https://signatone.com/high-power-stations/
5. https://www.lakeshore.com/products/categories/material-characterization-products/cryogenic-probe-stations

KEYWORDS: High Voltage, High Power, Wafer Probe System, Characterization, Reliability

DMEA241-003 TITLE: Ultra-High Voltage Reliability Test System

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: Develop an ultra-high voltage package-level reliability test system to conduct High Temperature Gate Bias (HTGB), High Temperature Reverse Bias (HTRB), High Humidity High Temperature Reverse Bias (H3TRB), and Accelerated Life Test High Temperature Reverse Bias (ALT-HTRB) testing for wide bandgap semiconductor devices. The package-level reliability test system shall be suitable for wide bandgap devices possessing a blocking voltage up to 40kV, including metal-oxide-semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors, (IGBTs), thyristors, and diodes.

DESCRIPTION: The growing popularity of high voltage, high power electronics in the commercial and defense industry is driving the need to perform reliability and qualification testing at ultra-high voltage and power levels. While many standards exist (i.e., JEDEC, IEC, MIL-STD, etc.) [2, 3], package-level reliability test systems capable of meeting the environmental and power requirements are commercially unavailable [4, 5].

For discrete wide bandgap devices, HTGB, HTRB, H3TRB, and ALT-HTRB are some of the primary reliability tests industry has adopted for qualifying device robustness. These tests require a temperature-humidity test chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration. The chamber must be capable of providing controlled conditions of temperature and relative humidity during ramp-up to, and ramp-down from, the specified test conditions [2, 3].

Currently, a package-level reliability test system capable of conducting HTGB, HTRB, H3TRB, and ALT-HTRB up to 40kV is not commercially available. Laboratories conducting these tests at high voltage levels must piece together measurement hardware and develop custom control software, leading to an increase in development costs and time [1].

The proposed package-level reliability test system seeks to integrate the required power supplies, measurement hardware, and control software into one cohesive system. To facilitate high volume testing, the proposed test system shall be capable of testing 80 devices simultaneously. The proposed package-level reliability test system shall be suitable for wide bandgap devices possessing a blocking voltage up to 40kV and gate threshold voltage (when applicable) of ±50V. The test system shall provide temperature control from 25C to 200C, and relative humidity control from 15% to 85%. The test system shall be capable of providing electrical connections to the devices under test for various high voltage packaging schemes.

PHASE I: Perform a feasibility study on the package-level reliability test system architecture as it relates to the requirements outlined in the preceding section of this document. The end product of Phase I is a feasibility study report, which demonstrates the proposed techniques for achieving the test system

requirements and justification for utilizing the proposed techniques. The report will explicitly address the following items:

1. Voltage Requirement: The feasibility study shall describe the proposed technique for achieving a target voltage rating of 40kV.
2. Temperature Requirement: The feasibility study shall describe the proposed technique for achieving a temperature-controlled environment of 25C to 200C.
3. Humidity Requirement: The feasibility study shall describe the proposed technique for achieving a humidity-controlled environment of 15% to 85%.
4. Package Adaptability: The feasibility study shall describe the proposed technique for adapting various high voltage packaging schemes into the test environment.
5. Control Software Requirement: The feasibility study shall describe the proposed technique for implementing the control software. The control software shall include programmable settings such as applied reverse voltage, gate voltage, stress time, current compliance, voltage compliance, and measurement readout options (e.g., threshold voltage Vth and leakage current).
6. Modular Design Requirement: The feasibility study shall describe the proposed technique for enabling a modular design, where components are swappable for replacement as equipment wears out.
7. Safety Requirements: The feasibility study shall describe the proposed technique for integrating high voltage interlock features and ensuring operator safety.

Respondents shall deliver a report that satisfies all of the requirements outlined in Phase I. If any of the above items cannot be fully addressed in the Phase I feasibility report, the report must include relevant research and justification for their inapplicability.

PHASE II: Phase II will result in the delivery of a fully functional prototype developed in Phase I. The prototype shall undergo rigorous testing to ensure its functionality and safety. This includes various experiments to evaluate its performance under different temperature and humidity conditions.
The complete test system architecture shall be documented into a final report. The final report must contain sufficient technical details on the system architecture, including circuit diagrams, schematics, bill of materials, and specifications. In addition, the final report must include details on the control software, its implementation, and a user guide. Finally, the final report must include details on the mitigated challenges that occurred during the development of the test system. Once completed, the fully functional prototype shall be delivered to DMEA for evaluation of the completed test system.
In addition to the fully functional prototype, a technical manual for operator-level maintenance and support shall constitute a deliverable. The technical manual shall include details for performing routine maintenance and debugging common issues.

PHASE III DUAL USE APPLICATIONS: : Phase III will conclude with the delivery of a fully developed and verified pre-production Ultra-High Voltage Reliability Test System capable of meeting all the performance specifications described in the preceding sections of this document. During the Phase III program, offerors may refine the performance of the test system. A pre-production unit with any and all refinements must be provided for evaluation.

During the Phase III program, offerors shall seek the appropriate regulatory certification to ensure product safety requirements are met. Offerors shall consider UL/IEC regulation at this stage for future commercialization. UL/IEC regulatory certification ensures that the test system meets the necessary safety standards and guidelines, which is vital for successful commercialization.

REFERENCES:

1. D. Berning, A. Hefner, J. M. Ortiz-rodriguez, C. Hood and A. Rivera, "Generalized Test Bed for High-Voltage, High-Power SiC Device Characterization," Conference Record of the 2006 IEEE

Industry Applications Conference Forty-First IAS Annual Meeting, Tampa, FL, USA, 2006, pp. 338-345, doi: 10.1109/IAS.2006.256543.
2. JEDEC, “Steady-State Temperature-Humidity Bias Life Test”, JESD22-A101D.01, JEDEC Solid State Technology Association, 2022, https://www.jedec.org/standards-documents
3. JEDEC, “Temperature, Bias, and Operating Life”, JESD22-A108G, JEDEC Solid State Technology Association, 2021, https://www.jedec.org/standards-documents
4. https://accelrf.com/solutions/htrb-multi-channel-test-system/
5. https://qualitau.com/category/special-applications/high-voltage-htrb-h3trb/

KEYWORDS: Silicon Carbide; SiC; HTRB; HTGB; Ultra-High Voltage; UHV; Package Test System; Reliability