DMEA
23.1 Small Business Innovation Research (SBIR)
Direct to Phase II Proposal Submission Instructions

INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR/STTR Program is implemented, administrated, and managed by the DMEA Office of Small Business Programs (OSBP). Proposers responding to a topic in this BAA must follow all general instructions provided in the Department of Defense (DoD) SBIR Program BAA. DMEA requirements in addition to or deviating from the DoD Program BAA are provided in the instructions below.

Specific questions pertaining to the administration of the DMEA SBIR/STTR Program and these proposal preparation instructions should be directed to the DMEA Acting SBIR/STTR Program Manager (PM), Mr. Tien Dang, at osd.mcclellan-park.dmea.list.smbus@mail.mil.

DIRECT TO PHASE II PROPOSAL GUIDELINES

15 U.S.C. §638 (cc), as amended by NDAA FY2012, Sec. 5106, and further amended by NDAA FY2019, Sec. 854, PILOT TO ALLOW PHASE FLEXIBILITY, allows the Department of Defense to make an award to a small business concern under Phase II of the SBIR program with respect to a project, without regard to whether the small business concern was provided an award under Phase I of an SBIR program with respect to such project. DMEA is conducting a "Direct to Phase II" implementation of this authority for this 19.2 SBIR Announcement and does not guarantee Direct to Phase II opportunities will be offered in future Announcements. Each eligible topic requires documentation to determine that Phase I feasibility described in the Phase I section of the topic has been met.

The DMEA SBIR Program reserves the right to not make any awards under this Direct to Phase II solicitation. The Government is not responsible for expenditures by the offeror prior to award of a contract. All awards are subject to availability of funds and successful negotiations.

The DMEA SBIR Direct to Phase II Proposals are different than traditional SBIR Phase I topics and proposals.

Direct to Phase II proposals must follow the steps outlined below:

STEP 1:
1. Offerors must create a Cover Sheet per the DOD SBIR 23.1 BAA instructions. Offerors must provide documentation that satisfies the Phase I feasibility requirement that will be included in the Supporting Documents (Volume 5) area of the Phase II proposal. Offerors must demonstrate that they have completed research and development through means other than the SBIR/STTR program to establish the feasibility of the proposed Phase II effort based on the criteria outlined in the topic description.

STEP 2:
1. Offerors must submit a Phase II proposal using the DMEA Phase II proposal instructions below.
2. The Phase II proposal must be submitted by the deadline as outlined in the the DOD SBIR 23.1 BAA instructions.

Offerors are required to provide information demonstrating that the scientific and technical merit and feasibility has been established. DMEA will not evaluate the offeror's related Phase II proposal if it determines that the offeror has failed to demonstrate that technical merit and feasibility has been

established or the offeror has failed to demonstrate that work submitted in the feasibility documentation was substantially performed by the offeror and/or the principal investigator (PI).

Refer to the Phase I description (within the topic) to review the minimum requirements that need to be demonstrated in the feasibility documentation. Feasibility documentation MUST NOT be based on work performed under prior or ongoing federally funded SBIR or STTR work.

PHASE II PROPOSAL GUIDELINES
Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

Phase II proposals may be submitted for an amount not to exceed $1,315,219.00 (excludes Discretionary Technical and Business Assistance (TABA) amount). The technical period of performance for the Phase II effort should be no more than twenty-four (24) months.

All Phase II proposals must have a complete electronic submission per the Proposal Volumes area listed below. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be considered for award.

Due to limited funding, DMEA's ability to award any Phase II, regardless of proposal quality or merit, is subject to availability of funds. Please ensure that your proposal is valid for 120 days after submission, and any extension to that time period will be requested by the contracting officer.

Any follow-on Phase II proposal (i.e., a second Phase II subsequent to the initial Phase II effort) shall be initiated by the Government Technical Point of Contact for the initial Phase II effort and must be approved by the DMEA SBIR/STTR Program Manager in advance.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please ensure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PROPOSAL VOLUMES:

Cover page (Volume 1)
Required per the DOD SBIR 23.1 BAA instructions.

Technical Volume (Volume 2)
The technical volume is not to exceed 40 pages and must follow the formatting requirements provided in the DoD SBIR Program BAA.

> **Content of the Technical Volume**
> Read the DOD SBIR Program BAA FY 23.1 for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be entertained.

DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DOD SBIR Program BAA FY 23.1 Preface Instructions. Due to limited funding, DMEA reserves the right to limit awards under any topic, and only proposals considered to be of superior quality will be funded.

Cost Volume (Volume 3)

DMEA does not accept Phase II proposals exceeding $1,315,219.00. DMEA will conduct a price analysis to determine whether cost proposals, including quantities and prices, are fair and reasonable. Contractors should expect that cost proposals will be negotiated. Costs must be separated and clearly identified on the Proposal Cover Sheet (Volume 1) and in Volume 3.

The on-line cost volume for Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a. through h. below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a. through h. below) as an appendix in your technical proposal. The itemized cost volume information (a. through h. below) will not count against the 40-page limit on Phase II proposal submissions.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting Officer, be advantageous to the government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DOD Component; unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DOD Component.

b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.

c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include teased hardware, must provide an adequate lease *versus* purchase justification or rationale.

d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.

e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.

f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.

g. Subcontracts: Involvement of university or other consultants in the planning and /or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by

the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.

h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

Please review the updated Percentage of Work (POW) calculation details included in section 5.3 of the DoD Program BAA. DMEA will not accept any deviation to the POW requirements.

Company Commercialization Report (CCR) (Volume 4)
Completion of the CCR as Volume 4 of the proposal submission in DSIP is required. Please refer to the DoD SBIR Program BAA for full details on this requirement. Information contained in the CCR will be considered by DMEA during proposal evaluations.

Supporting Documents (Volume 5)
Supporting documents will include the following:

Feasibility Documentation
a) Maximum page length for feasibility documentation is 20 pages. If you have references, include a reference list or works cited list as the last page of the feasibility documentation. This will count towards the page limit.

b) Work submitted within the feasibility documentation must have been substantially performed by the offeror and/or the principal investigator (PI). Technology in the feasibility documentation is subject to intellectual property (IP) rights, the offeror must provide IP rights assertions. Provide a good faith representation that you either own or possess appropriate licensing rights to all IP that will be utilized under your proposal. Additionally, proposers shall provide a short summary for each item asserted with less than unlimited rights that describes the nature of the restriction and the intended use of the intellectual property in the conduct of the proposed research. Please see the SBIR 23.1 BAA instructions for information regarding technical data rights.

Fraud, Waste and Abuse Training (Volume 6)
Fraud, Waste and Abuse (FWA) training is required for Phase I and Direct to Phase II proposals. Please refer to the DoD 23.1 SBIR BAA for full details.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM
To encourage transition of SBIR into DOD systems, DMEA has a Phase II Enhancement policy. DMEA's Phase II Enhancement program requirements include: up to one-year extension of existing Phase II, and up to $657,610.00 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

DISCRETIONARY TECHNICAL AND BUSINESS ASSISTANCE (TABA)
DMEA does not provide Discretionary Technical and Business Assistance (TABA).

EVALUATION AND SELECTION

All proposals will be evaluated in accordance with the evaluation criteria listed in the DoD SBIR Program BAA. Proposing firms will be notified of selection or non-selection status for a Phase II award within 90 days of the closing date of the BAA.

DMEA SBIR 23.1 Direct to Phase II Topic Index

DMEA231-D01 TITLE: Low Cost, High Power, Opening and Closing Switches

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics, Directed Energy

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: Develop low cost, high power, semiconductor opening switches (SOS), fast ionization dynistor (FID), or reverse switching dynistor (RSD) with an emphasis on being able to produce these devices at volume production facilities.

DESCRIPTION: Semiconductor opening and closing switches (SOS, FID, and RSD) are used for a variety of pulsed power systems and high-power microwave (HPM) systems for providing high peak power and repetition rates [1, 2]. While silicon drift step recovery diodes (DSRD) have been demonstrated and produced in limited quantities over the past several years, the related devices have not [3]. The final product should be stackable in order to achieve higher voltage and current. The drawback with stacked devices are internal inductance, capacitance, and resistance increasing and creating unwanted effects on the circuit. Most recently, research has been done on wide bandgap materials which has shown higher performance [4, 5]. However, this topic will focus on single device performance and cost. Prototypes and tests will be done on both single device and stacked devices.

The U.S. does not have a manufacturing source for many semiconductor opening and closing switches. Dopant concentration and junction depths are important factors for producing these devices. Preferably, proposed SOS, FID, or RSD devices can be produced in existing commercial semiconductor fabrication facilities without any additional capital costs. Ideally, the manufacturing process will be done on at least 6” substrates to facilitate volume production and with highly controllable process techniques without requiring near substrate melting point processing or multi-day processing steps, which is required for optimum silicon (Si) based DSRDs. Additionally, costs per device must be kept low in order to allow for broad adaptation.

Silicon carbide (SiC) based DSRDs have been investigated and proven superior in performance to Si based DSRDs [6, 7]. For similar reasons, SiC based SOS, FID, and RSD devices are of interest [8]. However, SiC substrates are known to be much more expensive compared to Si substrates and may impact the total cost for the device. Cost vs. performance tradeoffs will be considered.
Ideal minimum single device characteristics for an opening switch:

1. Breakdown voltage: >800V with full width at half maximum (FWHM) <1 ns or >600V with FWHM <5 ns
2. Peak Repetitive Operating current: 25 A / mm^3
3. Pulse repetition frequency: 100 kHz (static) to (1 MHz) dynamic
4. Switching time (transition or snap time): <1 ns for 80ns or <3.5 ns for 200ns of pumping time
5. Differential voltage (-dV/dt): 2kV/ns
6. Stackable design with low resistance loss
7. Form factor: circular with a diameter of 0.25”-0.8”
8. Cost: ≤ $100 per single device or ≤ $2,040 per delivered stack with 10kV of breakdown voltage

a. If in a stacked form factor, the added cost for stacking multiple individual devices to form a stack does not increase the final deliverable stack cost by more than 20%. An example 10kV stack might require 17 devices (10kV divided by 600V); however, it should cost no more than $2,040 delivered (17 devices multiplied by $100 increased by 20%).

Ideal minimum single device characteristics for a closing switch:

1. Breakdown voltage: >4kV static (1 second) and >6kV dynamic with 5 ns FWHM input
2. Pulse repetition frequency: 100 kHz (static) to (1 MHz) dynamic
3. Switching time (turn on time): <1 ns
4. Differential voltage (-dV/dt): 4-6kV/ns
5. Stackable design with low loss
6. Form factor: circular with a diameter of 0.25”-0.8”
7. Cost: ≤ $100 per single device, if in a stacked form factor, the added cost for stacking does not increase the final deliverable device by 20%. See the example in the opening switch section above.

DIRECT TO PHASE II: DMEA will only accept Direct to Phase II proposals.

PHASE I: Perform a feasibility study on designing, modeling, manufacturing, and characterizing one of the following types of devices: SOS, FID, or RSD. The end result of Phase I is a feasibility study report justifying the rationale supporting the proposed device and manufacturing process. Additionally, depending on the material used, high power devices can generate a lot of heat that can easily degrade the lifespan or performance of a device and thermal management can become an issue. Respondents should include a plan to evaluate and mitigate heat generation. Thermal management can be mitigated by material selection, but respondents must investigate and address this as part of the feasibility study report. Ideal minimum device characteristics allows proposals an opportunity to balance cost vs. performance.

The report will explicitly address the following items:
1. The feasibility study shall state which proposed device will be produced and whether it is intended as an opening or closing switch.
2. The feasibility study shall describe modeled characteristics and performance along with relevant figures, equations, and input parameters. It must include:
    a. Breakdown voltage (static and dynamic)
    b. Peak repetitive operating current
    c. Pulse repetition frequency
    d. Switching time
    e. Differential voltage (-dV/dt)
    f. Differential current (dI/dt)
    g. Temperature range (storage range and operating range)
    h. Form factor size and shape
    i. Number of devices needed to be stacked together to reach a dynamic breakdown voltage of 10kV along with performance characteristics of a 10kV stack
    j. Max number of stacked devices before thermal management is required, as well as the analysis that supports this conclusion
3. The feasibility study shall detail the process and techniques used along with associated costs. If there are bulk quantity discounts factored in, the report shall disclose quantity price break points and which steps were discounted where relevant. It is acceptable if proposed initial cost is higher than ideal; however, the proposal must detail a viable plan to scale costs to a competitive rate along with the order quantities required in order to achieve price break. It must include:
    a. Proposed manufacturing process flow and techniques used, including dicing, stacking, and packaging methodologies

b. Bulk material and specification (i.e., crystal orientation, dopant species, resistivity, thicknesses, etc.)
c. Cost break down for manufacturing comparison versus existing (both commercial and research) and comparative theoretical options. Table format preferred.
d. Methodologies and analysis techniques used for characterizing the proposed device (i.e., junction depth, doping profile, electrical performance, etc.)
e. Thermal management solutions for heat generated if or when thermal management is required

The delivered report must fully describe the proposed techniques and characterization methodologies, including a notional list of fabrication tools, facility requirements, and a program plan for follow-on phase development. The report must describe the tradeoff considerations done to meet cost and minimum device specs. If any of the above items cannot be fully addressed, the report must include relevant research and rationale that demonstrates their inapplicability to the proposed technique. If adhering to the above items is possible, but not financially feasible, the report must include relevant justification.

FEASIBILITY DOCUMENTATION: Offerors interested in participating in Direct to Phase II must include in their response to this topic, Phase I feasibility documentation that substantiates the scientific and technical merit and Phase I feasibility described in Phase I above has been met (i.e., the small business must have performed Phase I-type research and development related to the topic, but from non-SBIR funding sources) and describes the potential commercialization applications. The documentation provided must validate that the proposer has completed development of technology as stated in Phase I above. Documentation should include all relevant information including, but not limited to: technical reports, test data, prototype designs/models, and performance goals/results. Work submitted within the feasibility documentation must have been substantially performed by the offeror and/or the principal investigator (PI).

PHASE II: Based on the aforementioned study and applicable development/innovation, Phase II will result in producing fully functioning prototypes of either a SOS, FID, or RSD device as described in Phase I. Test and deliver the prototype, characterization results, all generated files (i.e., process recipes, process specifications, etc.), operating instructions, and test plans to the Government for further testing and verification. If the prototype does not meet the minimum requirements listed as described in Phase I, rationale must be provided for each parameter specification not met and a remediation strategy must be presented.

Required Phase II deliverables must include:
1. Validated characterization results verifying that ten (10) single device form factor prototype devices met the specifications as described in Phase I.
2. Validated characterization results demonstrating the performance of five (5) stacked devices. Each stack must reach a dynamic breakdown voltage of 10kV. Stacked device performance and characteristics results shall be reported in a similar format as the single device form factor.
3. At least fifty (50) untested, unpackaged, single device form factor samples and at least ten (10) untested, unpackaged, pre-diced wafers for further testing and validation.

The final report must reflect that the tested prototypes were selected from across multiple lots to demonstrate repeatability and quality with low variation within wafer, wafer to wafer, and lot to lot. If a non-random selection was required to optimize performance, the final report must detail reasoning for using non-random selection and the selection criteria used.

Deliver a detailed final report that documents the cost breakdown per single form factor, cost breakdown per stacked device, manufacturing processes utilized, fabrication toolset required to perform the proposed techniques, all facility requirements, all electrical characterization and device design data (TCAD files,

modeling/simulation, etc.), and diffusion profile results (i.e,. SRP). If there are bulk quantity discounts factored in any of the cost breakdowns, the final report shall disclose quantity price break points and which steps were discounted where relevant. The final report shall contain sufficient technical detail such that an entity skilled in semiconductor fabrication can repeat the presented results to the same level of performance.

PHASE III DUAL USE APPLICATIONS: There may be opportunities for further development of semiconductor opening and closing switches for use in a specific military or commercial application. During Phase III, offerors may refine the performance of the design and produce pre-production quantities for evaluation by the Government. Semiconductor opening and closing switches have commercial and Government applications. Pulsed power application examples include electron accelerators, X-ray pulse devices, high-power microwave electronics, pumping of gas lasers, ignition of electrical discharges, engine ignition, and ion implantation [9, 10].

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KEYWORDS: Drift Step Recovery Diode, DSRD, Semiconductor Opening Switch, SOS, Fast Ionization Dynistor, FID, Reverse Switching Dynistor, RSD, Pulse Repetition Frequency, PRF; High Power Microwave, HPM, Solid State, Ultra-Wideband, UWB.

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DMEA231-D02 TITLE: Ultra-High Voltage Insulated Gate Bipolar Transistor on Silicon Carbide

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: Develop an ultra-high voltage (UHV) insulated gate bipolar transistor (IGBT) on silicon carbide (SiC) technology with high reliability and yield so that these devices may be produced in a high volume manufacturing setting.

DESCRIPTION: Despite nearly three decades of research and development (R&D) efforts into SiC power devices, commercial SiC power transistors with voltage ratings greater than 1.7kV are not widely available. Despite significant R&D investments, a fully-qualified, commercially-available, greater than 6.5kV rated SiC power transistor has remained elusive [1-7]. On the other hand, there is an increased demand for UHV SiC power transistors, especially SiC IGBTs, for mission critical applications in both defense and commercial sectors. Other semiconductor materials (e.g., GaN) have been studied for their applicability in the UHV market, yet SiC has emerged as the material of choice for its UHV capabilities and enhanced thermal conductivity [2, 3, 5].

At present, there are very few manufacturing sources within the U.S. that can produce UHV SiC technologies [2, 5]. In addition, the manufacturing challenges associated with UHV SiC devices has hindered its adoption and advancement in the semiconductor industry. For example, in order to achieve ultra-high blocking voltages (e.g., >15kV), manufacturers must produce or procure SiC substrates with ultra-thick (>100um) SiC epilayers [3 – 7]. Ultra-thick SiC epilayers suffer from high basal plane defect (BPD) levels, especially if appropriately thick (>3um) buffer layers are not employed in the epi structure [5]. It is extremely important to tightly control the density of BPDs in the epilayers procured for device fabrication. It is imperative that an UHV SiC power transistor be developed to meet the UHV and switching speed requirements in mission critical systems. A SiC IGBT is an ideal candidate to meet this demand signal.

The proposed SiC IGBT must be produced on 150mm SiC substrates to facilitate high volume manufacturing, demonstrate a blocking voltage greater than 20kV, possess a current rating of at least 15A, threshold voltage Vth ~3.0V, and <500ns switching times at 80% of rated breakdown voltage. Form factor, ideally, will be 49mm2.

DIRECT TO PHASE II: DMEA will only accept Direct to Phase II proposals.

PHASE I: Perform a feasibility study on the selected fabrication process to obtain the device characteristics outlined in the preceding section of this document. The end product of Phase I is a feasibility study report, which demonstrates the proposed techniques, manufacturing process steps, and justification for utilizing the proposed techniques. The report will explicitly address the following items:

1. The feasibility study shall describe the proposed technique for obtaining global and local epitaxial layer flatness.

2. The feasibility study shall describe the substrate back grinding process for ohmic contact formation.
3. The feasibility study shall describe the method for enhancing carrier lifetimes in the N-drift layer, which is necessary for achieving a low VCE-SAT [5].
4. The feasibility study shall describe the utilization and role of modeling and simulation in the development of the proposed techniques.
5. The feasibility study shall describe all required fabrication tools utilized to implement the proposed techniques and describe each tools applicability to the manufacturing process.

Respondents shall deliver a report that satisfies all of the requirements outlined in Phase I. If any of the above items cannot be fully addressed in the Phase I feasibility report, the report must include relevant research and justification for their inapplicability.

PHASE II: Phase II will result in manufacturing, testing, and delivering a fully functional prototype of the SiC IGBT developed in Phase I. A thorough analysis of the devices' physical and electrical characteristics must be demonstrated by way of simulation. In conjunction, verification of the simulation results must be demonstrated by direct measure of the prototype device. The simulated and measured data that prove prototype conformance shall constitute a deliverable item and must be integrated into a final report. The final report must also contain sufficient technical details on the manufacturing process, mitigated challenges, and reliability of the device.

PHASE III DUAL USE APPLICATIONS: Phase III will conclude with the delivery of a fully developed and verified pre-production SiC IGBT capable of meeting all of the performance and process metrics described in the preceding sections of this document. During Phase III, offerors may refine the performance of the design or manufacturability of the component. A pre-production device with any and all refinements must be provided for evaluation.

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