Defense Microelectronics Activity (DMEA)
23.1 Small Business Innovation Research (SBIR)
Proposal Submission Instructions

INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR/STTR Program is implemented, administrated, and managed by the DMEA Office of Small Business Programs (OSBP). Proposers responding to a topic in this BAA must follow all general instructions provided in the Department of Defense (DoD) SBIR Program BAA. DMEA requirements in addition to or deviating from the DoD Program BAA are provided in the instructions below.

Specific questions pertaining to the administration of the DMEA SBIR/STTR Program and these proposal preparation instructions should be directed to the DMEA Acting SBIR/STTR Program Manager (PM), Mr. Tien Dang, at osd.mcclellan-park.dmea.list.smbus@mail.mil.

PHASE I PROPOSAL GUIDELINES

The Defense SBIR/STTR Innovation Portal (DSIP) is the official portal for DoD SBIR/STTR proposal submission. Proposers are required to submit proposals via DSIP; proposals submitted by any other means will be disregarded. Detailed instructions regarding registration and proposal submission via DSIP are provided in the DoD SBIR Program BAA.

DMEA intends for Phase I to be only an examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding $197, 283.00. The technical period of performance for the Phase I effort should be no more than six (6) months.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please ensure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PROPOSAL VOLUMES:

Proposal Cover Sheet (Volume 1)

Required per the DoD SBIR Program BAA.

Technical Volume (Volume 2)

The technical volume is not to exceed 20 pages and must follow the formatting requirements provided in the DoD SBIR Program BAA.

Content of the Technical Volume

Read the DoD SBIR Program BAA for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be accepted.

DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DoD SBIR Program BAA. Due to limited funding, DMEA reserves the right to

limit awards under any topic, and only proposals considered to be of superior quality will be funded.

Cost Volume (Volume 3)
DMEA does not accept Phase I proposals exceeding $197,283.00. DMEA will conduct a price analysis to determine whether cost proposals, including quantities and prices, are fair and reasonable. Contractors should expect that cost proposals will be negotiated. Costs must be separated and clearly identified on the Proposal Cover Sheet (Volume 1) and in Volume 3.

The on-line cost volume for Phase I and Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a. through h. below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a. through h. below) as an appendix in your technical proposal. The itemized cost volume information (a. through h. below) will not count against the 20-page limit on Phase I and II proposal submissions.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting Officer, be advantageous to the Government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DoD Component; unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DoD Component.

b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.

c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include teased hardware, must provide an adequate lease *versus* purchase justification or rationale.

d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.

e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.

f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.

g. Subcontracts: Involvement of university or other consultants in the planning and /or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost

Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.

h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

Please review the updated Percentage of Work (POW) calculation details included in section 5.3 of the DoD Program BAA. DMEA will not accept any deviation to the POW requirements

Company Commercialization Report (CCR) (Volume 4)
Completion of the CCR as Volume 4 of the proposal submission in DSIP is required. Please refer to the DoD SBIR Program BAA for full details on this requirement. Information contained in the CCR will be considered by DMEA during proposal evaluations.

Supporting Documents (Volume 5)
Other than the Volume 5 requirements listed in the DoD SBIR Program BAA, supporting documents are not required and will not be evaluated.

Fraud, Waste and Abuse Training (Volume 6)
Fraud, Waste and Abuse (FWA) training is required for Phase I and Direct to Phase II proposals. Please refer to the DoD SBIR Program BAA for full details.

PHASE II PROPOSAL GUIDELINES
Phase II proposals may only be submitted by Phase I awardees. Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

The Technical Volume is not to exceed 40 pages and consists of a single PDF file with your firm name, topic number, and proposal number in the header of each page. All documentation should use no smaller than 10 point font on standard 8.5" X 11" paper with one-inch margins and not be in two-column format. Do not include blank pages.

Phase II proposals may be submitted for an amount not to exceed $1,315,219.00. The technical period of performance for the Phase II effort should be no more than twenty-four (24) months.

Phase I awardees may submit a Phase II proposal without invitation not later than sixty (60) calendar days following the end of the Phase I contract. The Phase II proposal submission instructions are identified in the Phase I contract, Part I – The Schedule, Section H, Special contract requirements, “SBIR Phase II Proposal Submission Instructions.”

All Phase II proposals must have a complete electronic submission per the Proposal Volumes area listed in Phase I. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be considered for award.

Due to limited funding, DMEA’s ability to award any Phase II, regardless of proposal quality or merit, is subject to availability of funds. Please ensure that your proposal is valid for 120 days after submission, and any extension to that time period will be requested by the Contracting Officer.

A Phase II contractor may receive up to one additional, sequential Phase II award for continued work on a project. The additional, sequential Phase II award has the same guideline amounts and limits as an initial

Phase II award. Sequential, Phase II proposals shall be initiated by the Government Technical Point of Contact for the initial Phase II effort and must be approved by the DMEA SBIR/STTR Program Manager in advance.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM

To encourage transition of SBIR into DoD systems, DMEA has a Phase II Enhancement policy. DMEA's Phase II Enhancement program requirements include: up to one-year extension of existing Phase II, and up to $657,610.00 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

DISCRETIONARY TECHNICAL AND BUSINESS ASSISTANCE (TABA)

DMEA does not provide Discretionary Technical and Business Assistance (TABA).

EVALUATION AND SELECTION

All proposals will be evaluated in accordance with the evaluation criteria listed in the DoD SBIR Program BAA. Proposing firms will be notified of selection or non-selection status for a Phase I or Phase II award within 90 days of the closing date of the BAA.

Refer to the DoD SBIR Program BAA for procedures to protest the Announcement. As further prescribed in FAR 33.106(b), FAR 52.233-3, Protests after Award should be submitted to:

DMEA Acting SBIR/STTR Program Manager (PM):

- Name: Mr. Tien Dang
- Email: osd.mcclellan-park.dmea.list.smbus@mail.mil

DMEA SBIR 23.1 Topic Index

DMEA231-001 TITLE: High-G Accelerometers

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: The DoD is seeking the development of a low cost, military temperature rated (storage -55 C to 125 C; operational -40 C to 55 C), US-sourced, tri-axis accelerometer capable of surviving up to 60 kG. Current commercially available accelerometers survive up to 35 kG under test. The device shall have a 10μs low recovery time after being subjected to the shock environment. The device shall also seek to incorporate test modes and self-bias correction. The device shall be printed circuit board (PCB) surface mountable with a large central electrically conductive pad for mechanical stability and seek to minimize the overall footprint and volume to the maximum extent possible.

DESCRIPTION: Many fuzing applications for the DoD require the sensing and validation of unique launch environments in order to provide safety prior to arming a munition. Many of these munitions must not only survive harsh military environments, but also must survive and reliably function during and after high-G acceleration events associated with munition launch [1]. For given applications and specifications there are various accelerometer architectures with special attention to high-G accelerometers [2]. Prior work has been successful with silicon carbide (SiC) microelectromechanical systems (MEMS)-based solutions [3, 4]. Preferably, the proposed device can be produced in existing commercial MEMS fabrication facilities without any additional capital costs. Ideally, the manufacturing process will be done on at least 6” substrates to facilitate volume production. Ideally, full production devices will cost less than $100 per single device to customers.

PHASE I: Conduct a feasibility study and design of an accelerometer capable of surviving up to 60 kG. The methods and considerations for simulation of accelerometers in a high-G environment shall be described. Accelerometer architecture and methods of microfabrication shall be defended regarding the following application-based specifications:

1. In addition to the 60 kG survival specification, the accelerometer requires a typical recovery time of 10μs while exhibiting a zero shift no greater than 3%.
2. The accelerometer shall operate over the temperature range (-40 C to 55 C), with a temperature stability of less than or equal to 5mG/ºC and nonlinearity of +/- 1%.
3. The US Government is initially interested in an accelerometer working with a sense range of +/- 25 kG and a sensitivity resolution of 0.1mV/G.
4. The accelerometer shall have a cross axis sensitivity of less than or equal to 3% and a resonant frequency of greater than 18 kHz.
5. The accelerometer shall draw no more than 1 mA at 5 VDC.
6. The accelerometer shall have a turn on time of less than 1 ms.
7. The design of the accelerometer should also consider the US Government’s interests in accelerometers with +/- 1 kG, +/- 10 kG, and +/- 50 kG sense ranges.

The feasibility study shall detail the process and techniques used along with associated costs. If there are bulk quantity discounts factored in, the report shall disclose quantity price break points and which steps were discounted wherever relevant. In addition, it must include:

1. Proposed manufacturing processes flows and techniques used, including dicing and etching methodologies, along with figures and diagrams describing the process.
2. Bulk material and specification (i.e., crystal orientation, dopant species, resistivity, epi thickness if any, etc.).
3. Cost break down for manufacturing compared to existing (both commercial and research) and comparative theoretical options.
4. Methodologies and analysis techniques used for characterizing the proposed device (i.e., how will you demonstrate the device will survive a up 1G to 60kG event?).

The delivered report shall fully describe the proposed techniques and characterization methodologies, including a notional list of fabrication tools, facility requirements, and a program plan for follow-on phase development. If any of the above items cannot be fully addressed, the report must include relevant research and rationale that demonstrates their inapplicability to the proposed technique. If adhering to the above items is possible, but not financially feasible, the report must include relevant justification. Finally, the challenges and special considerations for testing of accelerometers under high-G stress environments shall be addressed.

Respondents shall deliver a report that satisfies all of the requirements outlined in Phase I. If any of the above items cannot be fully addressed in the Phase I feasibility report, the report must include relevant research and justification for their inapplicability.

PHASE II: Build, test and deliver a fully functional accelerometer based on the design developed in Phase I. Demonstrate the capability of surviving 60 kG while adhering to the specifications outlined in Phase I. Production yields shall be considered to keep costs low with commercialization a viable option. The final report shall address manufacturing yield and reflect that the tested prototypes were selected from across multiple lots to demonstrate repeatability and quality with low variation within wafer, wafer to wafer, and lot to lot. If a non-random selection was required to optimize performance, the final report must detail reasoning for using non-random selection and the selection criteria used.

Deliver a detailed final report that documents the cost breakdown per device, manufacturing processes utilized, fabrication toolset required to perform the proposed techniques, all facility requirements, and all electrical characterization and device design data (TCAD files, modeling/simulation results, etc.). If there are bulk quantity discounts factored in any of the cost breakdowns, the final report shall disclose quantity price break points and which steps were discounted where relevant. The final report shall contain sufficient technical detail such that an entity skilled in semiconductor fabrication can repeat the presented results.

PHASE III DUAL USE APPLICATIONS: This technology could be utilized for other DoD and commercial applications where high-G and repeated shock events may occur, such as On-Board Recorders (ORBs), flight termination systems, airline black box flight recorders, or crash test instrumentation.

REFERENCES:

1. T. G. Brown, “Harsh military environments and microelectromechanical (MEMS) device”, Proceedings of IEEE Sensors, vol 2, 2003;
2. V. Narasimhan et al, “Micromachined high-g accelerometers: a review,” J. Micromech. Microeng., vol 25, 2015;

3. Andrew Atwell et al, “Simulation, fabrication and testing of bulk micromachined 6H-SiC high-g piezoresitive accelerometers”, Sensors and Actuators, A 104, 2003;
4. Yanxin Zhai et al, “Design, fabrication and test of a bulk SiC MEMS accelerometer”, Microelectronic Engineering, 260, 2022

KEYWORDS: MEMS, Accelerometer, Transducer

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DMEA231-002 TITLE: High-G Clock Source

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: The DoD is seeking a high-G rated (100 kG), low power (< 1mA @ 3V), US sourced, ceramic resonator, microelectromechanical systems (MEMS) oscillator, or crystal oscillator. This resonator, or oscillator, shall be designed to work over the military temperature range (storage -55C to 125 C; operational -40 C to 85 C), survive shock greater than 100 kG, operate under 4 kG centripetal force, smaller than 4.5mm in area, and while operating in the 4 MHz to 19 MHz range.

DESCRIPTION: Fuzing applications that employ height of burst (HOB) sensors utilize either ceramic resonators or crystal oscillators to set the operating frequency and bandwidth of these systems. Historically, Ceramic Resonators were low cost, but with a large physical footprint which were acceptable for large munition HOB sensors. However, as fuzing technology is being applied to smaller munitions, the Ceramic Resonators are too large to accommodate the Size, Weight, Power, and Cost (SWaP-C) requirements while low cost crystal oscillators cannot meet the high-G rating of fuzing. Current applications show timing sources surviving peak acceleration forces of up to 65 kG for about 100us, after that the acceleration tails off exponentially. Having a clock source surviving up to 100 kG is desired. The sensitivity of quartz crystal oscillators to acceleration has been well documented [1]. Research on crystal oscillators has resulted in a quartz crystal oscillator that exhibited G-sensitivity (change in frequency resulting in acceleration force) of 2E-9/g [2]. Also, research on different MEMS oscillators have also shown low-G sensitivity [3, 4]. However, this topic requires development to be done on survival shock.

PHASE I: Define whether a ceramic resonator, MEMS oscillator or crystal oscillator will be investigated. Conduct a feasibility study and design of an oscillator capable of surviving up to 100 kG. The methods and considerations for simulation of oscillators in a high-G environment shall be described. The choice of oscillator architecture and methods of microfabrication shall be defended regarding the following application-based specifications:

1. 4 MHz to 20 MHz oscillating frequency, +/- 3000 ppm.
2. 10 ms maximum start-up time.
3. 100 kG survival specification, device is inactive at time of this shock.
4. +/- 2000 ppm oscillator drift over 10 years.
5. +/- 2000 ppm temperature coefficient.
6. Operational conditions: 2.7 to 3.6 V, -40 C to 85 C, 4000 G centripetal force conditions, with +/- 2000 ppm.
7. Current consumption: < 1mA at 3V, T = 25C.

The feasibility study shall detail the process and techniques used along with associated costs. If there are bulk quantity discounts factored in, the report shall disclose quantity price break points and which steps were discounted where relevant. In addition, it must include:

1. Proposed manufacturing processes flows and techniques used including dicing and etching methodologies, along with figures and diagrams describing the process.

2. Bulk material and specification (i.e., crystal orientation, dopant species, resistivity, epi thickness if any, etc.).
3. Cost break down for manufacturing compared to existing (both commercial and research) and comparative theoretical options.
4. Methodologies and analysis techniques used for characterizing the proposed device (i.e., how will you demonstrate the device will survive a 100 kG event, then operate under a 4 kG centripetal force?).

The delivered report shall fully describe the proposed techniques and characterization methodologies, including a notional list of fabrication tools, facility requirements, and a program plan for follow-on phase development. If any of the above items cannot be fully addressed, the report must include relevant research and rationale that demonstrates their inapplicability to the proposed technique. If adhering to the above items is possible, but not financially feasible, the report must include relevant justification. Finally, the challenges and special considerations for testing of oscillators under high-G stress environments shall be addressed.

Respondents shall deliver a report that satisfies all of the requirements outlined in Phase I. If any of the above items cannot be fully addressed in the Phase I feasibility report, the report must include relevant research and justification for their inapplicability.

PHASE II: Build, test and deliver a fully functional, printed circuit board (PCB)-mountable oscillator based on the design developed in Phase I. The clock source must be able to be potted (i.e., completely covered in non-conductive polyurethane). The units will not only be potted, but also be subjected to a vacuum on the electronics to remove air bubbles. Therefore, the device must either be hermetically sealed or be able to operate covered in the non-conductive polyurethane potting. Demonstrate the capability of surviving 100 kG while adhering to the specifications outlined in Phase I. Production yields shall be considered to keep costs low with commercialization a viable option. The final report shall address manufacturing yield and reflect that the tested prototypes were selected from across multiple lots to demonstrate repeatability and quality with low variation within wafer, wafer to wafer, and lot to lot. If a non-random selection was required to optimize performance, the final report must detail reasoning for using non-random selection and the selection criteria used.

Deliver a detailed final report that documents the cost breakdown per device, manufacturing processes utilized, fabrication toolset required to perform the proposed techniques, all facility requirements, and all electrical characterization and device design data (TCAD files, modeling/simulation results, etc.). If there are bulk quantity discounts factored in any of the cost breakdowns, the final report shall disclose quantity price break points and which steps were discounted where relevant. The final report shall contain sufficient technical detail such that an entity skilled in semiconductor fabrication can repeat the presented results.

PHASE III DUAL USE APPLICATIONS: Other applications of this technology would be for small, low-cost embedded RAdio Detection And Ranging (RADAR) sensors for Automotive Safety, Sports Equipment, or Industrial Safety applications (which typically run with clock rates < 10 MHz), where repeated shock events may occur.

REFERENCES:

1. Raymond Filler, “The Acceleration Sensitivity of Quartz Crystal Oscillators: A Review” IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, 1988.
2. M Bloch et al, “Acceleration ‘G’ Compensated Quartz Crystal Oscillators”, 2009 IEEE International Frequency Control Symposium Joint with the 22nd European Frequency and Time forum, 2009

3. Bongsang Kim et al, “MEMS Resonators with extremely low vibration and shock sensitivity”, IEEE Sensors, 2011
4. Beheshteh Najafabadi, “Study of Acceleration Sensitivity and Nonlinear Behavior in Silicon-based MEMS Resonators”, Doctoral Dissertation, University of Central Florida, 2019

KEYWORDS: MEMS Resonator, Crystal Oscillator

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DMEA231-003 TITLE: High Voltage Package Encapsulation using Innovative and Advanced Materials

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

OBJECTIVE: Development and characterization of new innovative encapsulation materials that are compatible with existing manufacturing methods, materials, and commercially available packages. Materials investigated shall be compared to the performance of established encapsulation materials used for high voltage power device packaging encapsulation. Investigation into the long-term stability of material performance when subjected to high temperatures (HT), high voltages (HV), wide frequency ranges, and high-pressure and humidity environments for packages intended for aircraft and spacecraft applications.

DESCRIPTION: The long-term stability of encapsulation material properties (electrical, morphological, chemical, and mechanical) is a key factor for whole system reliability under operational and environmental constraints [7]. Silicones and epoxies are typically considered for embedding, potting, and/or encapsulating HV/HT electronic assemblies [4]. Soft dielectric materials, such as silicone gel, are used to encapsulate modules and prevent electrical discharges in air, as well as, to protect semiconductors, substrates, and connections against humidity, dirt, and vibration [4]. Embedding materials must be characterized for use in these types of HV/HT electronic assemblies. A focus in the characterization is the dielectric strength, which is influenced by the following factors: environmental exposure, electrode effects, temperature, voltage application, frequency, and specimen width [3]. The mechanical stresses experienced by packages can also significantly influence the dielectric properties of polymeric dielectrics [5]. In more compact packaging technology for high-power density wide band gap (WBG) devices, the local electric field can be enhanced, which may become large enough to raise partial discharges (PD); localized gaseous breakdown within the modules insulation system [1]. High activity of PDs damages the insulating silicone gel, leading to electrical insulation failure and reduction in the reliability of the module [1]. Partial discharge that occurs in micro-voids will cause accelerated aging and early failure. Voids inside the silicone gel significantly accelerate the aging of the materials even under normal operating electrical stress [1]. For these reasons, emphasis has been placed on the partial discharge, aging, and electrical treeing of semiconductors' packaging material [6]. Partial discharge has been recognized as a suitable technique to assess polymeric materials for insulation applications along with High-Current Arc Resistance to Ignition (HAI); a method that studies and assesses the electrical insulation flammability [3].

Soft encapsulation materials play a significant role in improving both semiconductor die and module package voltage ratings, especially under enhanced electrical and thermal constraints, by isolating the circuits from the effects of impurities and avoided fractures from thermomechanical stresses [7][2]. A variety of material innovations have been explored thus far, but further characterization and development is required before new materials can be used in practice. Some material solutions that have been explored are composite materials that offer the opportunity to provide a suitable product with the final application's required performance, thereby optimizing the price-performance ratio [3]. The emergence of micro and nano-based inorganic oxide fillers with optimal filler-loadings further enhances the required insulation characteristics of neat epoxy [5]. Another route investigated was applying functional materials on the highly stressed regions to reduce the electric field and the use of dielectric liquids which are incompressible, to fill voids and exhibit a self-healing effect [1][2]. While methods for achieving long-term stability of package encapsulate material have been explored through several means, full performance characterization of any proposed material advancement with consideration of extreme service conditions (HV, HT, and high moisture) is required prior to fielded application in aircraft or spacecraft. Electronic devices in aircraft are expected to meet operating temperature on order of 250C-300C and spacecraft and nuclear power systems requirements are on order of 200C-400C [4].

Consideration of the material and material application to device compatibility with existing manufacturing techniques is critical to reduce imposed cost of implementing material solutions.

PHASE I: Perform a feasibility study of innovative or advanced materials that can be used for HT and HV applications in the field of aircraft and spacecraft, with consideration for characterizing the long-term stability of the material while exposed to HT, HV, various frequency ranges, and humid environments.

Develop a testing plan and methodology that considers to operation conditions of interest (i.e. temperatures above 250C up to 400C and high humidity conditions), as well as HAI and PDs. Materials of interest shall target the following performance specifications:

1. Material(s) must be capable of operating at a temperature of 250C minimum and targeting operational temperatures as high as 400C
2. Coefficient of thermal expansion (CTE) values shall target values similar to those of typical substrate materials that would interface with the encapsulation materials (such as Al2O3, Copper, BeO, etc.), which typically have CTE values around 10 to 7 10^-6/C
3. Pass MIL-STD-202 Humidity (Steady State) condition A
4. Pass UL 746A High Amp Arc Ignition test PLC 0
5. Adhesion to a wide variety of substrates including metals, composites, glass, ceramics, and plastics
6. Show compatibility with existing manufacturing techniques

PHASE II: Using the methods developed in Phase I, materials identified to be representative of current encapsulation materials and materials that could be applied to higher temperature (200C-400C) and higher operational voltages (5kV-20kV) shall undergo material characterization. Material performance characterization shall report performance in the following areas:

1. Electrical testing of material volume resistivity(ASTM D257), dielectric strength (ASTM D149), HAI and PD
2. Thermal testing to determine the coefficient of thermal expansion (CTE) (ASTM D696), conductivity (ASTMC177), and relative thermal index (UL 746).
3. Physical testing of heat deflection temperature and max service temperature
4. Material reliability in moisture or humid environments
5. The above tests shall also test for influence of voltage, frequency, environmental temperature and humidity have on material performance, stability and aging:
    a. Testing voltage ranges: 700V-1.7kV, 1.7kV-3.3kV, 3.3kV-10kV, 10kV-20kV, with a focus on the 10kV to 20kV range
    b. Stability under isothermal aging from: -40 up to 400C
    c. Frequencies up to 100kHz

The performer is expected to test to the above value ranges or conditions. If unable to do so, justification for excluding the data set must be demonstrated. The performer is expected to show repeatability in the data collected as well as deliver the testing data and samples for which the experiments were performed, as applicable.

PHASE III DUAL USE APPLICATIONS: The encapsulation materials developed can be marketed towards manufacturing and packaging industries and materials distributers for commercial application. Materials developed could be marketable toward DoD for use in DoD applications that are fielded in demanding environments/conditions. The material testing and characterization capability could also be marketed as a service to material design experts in industry.

REFERENCES:

1. Ghassemi, Mona. (2018). Electrical Insulation Weaknesses in Wide Bandgap Devices. 10.5772/intechopen.77657.

2. Abdelmalik, Abdelghaffar & Liland, K.B.. (2020). Electric field enhancement control in active junction of IGBT power module. Journal of Physical Science. 31. 1-15. 10.21315/jps2020.31.3.1.
3. Haque, S. K. Manirul et al. “Application and Suitability of Polymeric Materials as Insulators in Electrical Equipment.” Energies 14 (2021): 2758.
4. Hopkins, D.C. & Bowers, J.S.. (2001). Characterization of advanced materials for high voltage/high temperature power electronics packaging. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC. 2. 1062 - 1067 vol.2. 10.1109/APEC.2001.912498.
5. Iqbal, Muhammad & Khattak, Abraiz & Ali, Asghar & Ullah, Nasim & Alahmadi, Ahmad & Khan, Adam. (2021). Influence of Ramped Compression on the Dielectric Behavior of the High-Voltage Epoxy Composites. Polymers. 13. 3150. 10.3390/polym13183150.
6. Chen, Chi, et al. "Transport Characteristics of Interfacial Charge in SiC Semiconductor Epoxy Resin Packaging Materials." Frontiers in Chemistry (2022): 316.
7. Locatelli, Marie-Laure & Khazaka, Rabih & Diaham, Sombel & Pham, Cong Duc & Bechara, Mireille & Dinculescu, S. & Bidan, Pierre. (2014). Evaluation of Encapsulation Materials for High-Temperature Power Device Packaging. Power Electronics, IEEE Transactions on. 29. 2281-2288. 10.1109/TPEL.2013.2279997

KEYWORDS: High voltage, package encapsulation, high temperature, partial discharge, electronics

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DMEA231-004 TITLE: Modular Cryogenic Dewar for Radiation Testing

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Space Technology, Microelectronics

OBJECTIVE: To develop modular, open architecture, cryogenic-and-environmental-test Dewar system for radiation testing of microelectronics and other test articles.

DESCRIPTION: Failure mechanisms of microelectronics and other components in radiation environments, such as those encountered by spacecraft, are often enhanced by other environmental conditions (i.e., temperature, pressure, and humidity) [1]. Interaction between radiation parameters, such as Total Ionizing Dose and environmental parameters (i.e., temperature), can be nonlinear and difficult to predict. This necessitates radiation testing with Dewar temperature systems capable of providing a range of environments.

PHASE I: Develop a system architecture package including a system architecture plan and drawings for modules comprising fully capable system.
The system architecture plan shall define the module types comprising a fully capable system and their interfaces. The functionality, inputs, outputs, and characteristic design constraints on each module type shall be defined. Interfaces between modules shall be defined including data interfaces, software interfaces, power interfaces, fluid interfaces, physical connection and fasteners, clearances, materials requirements, and any other definitions required to specify drop-in modular designs. Commonly available and standard parts and protocols shall be used for module interfaces wherever possible. The system architecture plan shall include schematics for the system incorporating all module types without going into details internal to module design.

A fully capable system shall meet the following requirements:

1. Capable of exposing a device under test (DUT) to a vacuum range of 1E-06 torr to ambient
2. Maintain selected vacuum within accuracy of +/-1%
3. Attain 1.0E-06 torr from ambient pressure within 90 minutes of startup with no DUT present
4. Capable of heating a DUT to 200+/-1 degree Celsius from ambient temperature
5. Capable of cooling DUT to -150+/-1 degree Celsius from ambient temperature
6. Rate of heating and cooling of 1 degree Celsius per minute or more
7. Utilize only safe, non-reactive working fluids for temperature system
8. Capable of attaining a humidity range from 5 to 80% Relative Humidity (RH) +/-5% RH over a temperature range of 20 to 85 degrees Celsius and pressure range from 0 psig to 200 psig
9. Dew point differential shall be 3 degrees Celsius to prevent condensation in the DUT chamber
10. Control of system from front panels or by general purpose interface bus (GPIB) to a computer with control software
11. All environmental condition exposed hardware shall be rated for the listed temperatures, pressures, and humidity
12. Modules for insertion into irradiation chambers should have a weight of less than 50 pounds or, if over, as close as practicable
13. All materials and parts that will be exposed to radiation shall be capable of withstanding exposure to radiation to a level of 2.0E7 rad (material) without degradation during a two-hour exposure and shall be designed in such a manner that components which may degrade above 2.0E7 rad (material) can be replaced without special tooling
14. All chlorofluorocarbon compounds are prohibited
15. All polytetrafluoroethylene (PTFE or Teflon) is prohibited
16. Cooling lines shall be insulated over entire lengths subject to operator handling, such that a temperature range of 0 to 43 degrees Celsius is maintained

17. All pressurized components shall be designed with a burst Maximum Operating Pressure factor of safety of 4
18. Relief valves and rupture disks shall be included in pressurized modules
19. Vacuum seals shall be capable of achieving leakage < 1E-08 scc/sec of helium
20. Modules subject to irradiation will be constructed of low atomic number material to the extent practicable
21. Structural welds will be minimized for vacuum chambers
22. All stainless steel surfaces exposed to high vacuum shall be electropolished
23. The system shall be designed such that DUT modules and other irradiated modules may provide at least 12 square inches of surface area for feed-through installation of test interfaces and sensor interfaces. Actual module feed-through surface area may be less than 12 square inches
24. DUT module interface shall be such that the DUT module can be exchanged within 10 minutes by a trained operator, not including DUT fitting.

The module drawings included in Phase I shall fit these requirements in addition to fulfilling the system requirements:

1. Electrical control connector for DUT with 50 pins and a pin rating of not less than 250 volts and 10 amps
2. DUT module and any other modules to be inserted into the irradiation chamber shall not exceed 15 inches wide by 15 inches high by 17 inches in length
3. DUT module shall have lead dose enhancement shroud surrounding the module with minimal practicable openings. Lead thickness to be 1.5 to 2.0 mm [3].

PHASE II: Fabricate and validate a fully capable system with at least two DUT modules spares in addition to primary module. The system shall be validated with the following tests in addition to verification of all above requirements:

1. Acceptance proof testing to 300 psig
2. Vacuum seal leak test at <1E-08 scc/sec of helium after successfully cycling the thermal chamber at least 3 times from -150 to 200 degrees Celsius

PHASE III DUAL USE APPLICATIONS: The described Dewar system has dual use application for radiation testing for commercial space, medical radiology, and civilian nuclear applications. The same characteristics of quick setup, high availability, high serviceability, and flexibility would be attractive for these applications. Many of the same radiation test resources supporting DoD testing are utilized for these applications. Often congruity between test facilities is an important consideration for comparison, which a modular Dewar system could offer. Modules could be quickly designed for various test facilities and applications while using the same system architecture and reusing much of the same hardware.

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KEYWORDS: Cryogenic, Vacuum, Dewar, Radiation Testing, Total Ionizing Dose, Low Temperature, High Temperature, Environmental Test

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DMEA231-005 TITLE: Vertical Photoconductive Semiconductor Switch (PCSS) and Triggering Assembly

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: Develop vertical photoconductive semiconductor switches (PCSS), which are triggered by a suitable optical source(s). The vertical PCSS should be capable of sub-nanosecond switching and hold off the voltage in excess of 100 kV with the current at least 10 kA. The current conducts via simultaneous multiple current paths (filaments) formed through the bulk of the semiconducting material. Moreover, the jitter associated with multi-formation of current paths (filamentation) should not exceed 20 ps for providing simultaneous switching operations. Also, the objective assembly must have a suitable optical source driver for initiating the PCSS triggering process. Finally, efficient delivery and use of a minimum of optical energy for PCSS triggering are of paramount importance.

DESCRIPTION: Many conventional pulse-power systems need ultra-fast switching devices that can operate in high-voltage, high current regimes. A current popular lateral PCSS is normally triggered with above band-gap radiation, which is strongly absorbed (less than 1 micron absorption depth) and which can trigger filaments in a linear array parallel and close to the illuminated surface of the device (10-100 microns). On the other hand, when using sub-band-gap radiation with an exceptionally long absorption depth (many millimeters) to trigger a vertical PCSS, filaments can be formed through the thickness or depth of the device in a two-dimensional array. A 1 cm × 1 cm lateral PCSS with a linear array of filaments spaced 300 micrometers apart can support about 33 filaments and a total current which increases linearly with the width of the device. Therefore, the lateral PCSS structure limits total current, performance, and scales. However, the same surface area on a vertical PCSS can support over 1,000 filaments, and a total current which increases with the illuminated surface area of the device. A vertical PCSS, in which current is conducted in filaments perpendicular to the illuminated surface of the device, has an advantage over a lateral PCSS of supporting many more filaments and hence much higher total current per device. With vertical PCSS, the highest fields can be confined to the bulk substrate away from the surface, so higher fields may be held-off and an insulating liquid may not be required. In addition, more benefits with vertical structures are expected. An issue that reduces electric field hold-off is field enhancement at sharp boundaries of conductive and dielectric interfaces. In conventional lateral geometry switches, these sharp interfaces also induce current crowding where the filaments enter the contacts from the semiconductor, causing high current density-induced degradation of the contacts. The surface-normal filament geometry in the proposed vertical switch mitigates this issue, which, in addition to the 2-D scalability of the number of current-sharing filaments, further greatly increases the current-handling capability of the switch.

PHASE I: Conduct a feasibility study and design of a single vertical PCSS/Optical trigger assembly, which includes a suitable optical source driver. The design will include the choice of the semiconducting material (e.g, GaN, SiC, or GaAs), bulk topology/dimensions (thickness/length/width) and choice of contact materials, which must be CMOS process compatible. The design must assure high voltage (minimum 100kV), high-current (minimum 10kA) and low jitter (maximum 20 ps) operation. Optical

source may include a laser diode(s) or a stand-alone laser (potentially with optical micro-lenses to avoid wasting trigger light outside the optical apertures). While the proposed effort calls for a single vertical PCSS/trigger source assembly, the driver design should be scalable for supporting future synchronized multi-PCSS operation.

PHASE II: Build, test, and deliver a fully functional vertical PCSS/trigger source prototype based on the design developed in phase I. Demonstrate the capability to achieve a conduction current pulse width of more than 50 ns. Carry out experimentations in air and insulating liquid, such as Flourinert, in order to compare switch capabilities in two distinct media. Prototypes must be able to carry out a lifetime of 300 shots with the switching current in excess of 1kA.

PHASE III DUAL USE APPLICATIONS: The successful completion of Phase II effort will significantly enhance the performance of ultra-fast PCSSs enabling them to operate in a high-voltage, high-current pulse-power environment. Military applications include various fast switch-based microwave sources for directed energy systems, UWB (Ultra-Wideband) pulse sources, and ground penetration radar. Phase III will result in fabrication of a new generation of pulse-power directed energy systems in many areas supporting military and civilian tasks including counter UAS operations, remote immobilization of vehicles and boats, IED neutralization, and non-lethal area denial. In addition, the vertical PCSS can be utilized for the medical imaging technologies as well as Q-switches used in lasers, where high voltage, high current are required.

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KEYWORDS: PCSS, Vertical PCSS, Photoconductive Semiconducting Switch.

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DMEA231-006 TITLE: Ultra-Wideband Voltage Controlled Oscillator

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

OBJECTIVE: To ensure maximum adjustability and design reuse for different applications, the DoD is seeking a low power (< 30mA @ 3V), US-sourced, ultra-wideband voltage-controlled oscillator (VCO). This VCO shall be designed to work over the military temperature range (-55 C to 125 C). The VCO shall also seek to have a selectable operating range via programmable pins.

DESCRIPTION: Fuzing applications that employ height of burst (HOB) sensors utilize specialized chipsets that set the operating range and output power for these systems. Different applications require specific parameters given operational environments, input power, form factor, etc. To ensure maximum adjustability and design reuse for different applications, the DoD is seeking a low power (< 30mA @ 3V), US- sourced, ultra-wideband voltage controlled oscillator (VCO). This VCO shall be designed to work over the military temperature range (-55 C to 125 C). Much research has been done on VCO design and architectures to increase its figure of merit (FOMT) when considering frequency tuning range (FTR), power dissipation (PD) and phase noise (PN) [1,2], while exhibiting a tuning frequency range of 8.86-13.4 GHz [2]. Also, some research work has been done on VCOs with variable center frequency architectures and any performance tradeoffs associated with it [3].

PHASE I: Conduct a feasibility study of the design tradeoffs of an ultra-wideband VCO with a tunable frequency range of 4-12 GHz, (range, 2x the minimum frequency). State of the art VCOs typically exhibit a tunable range of about 1x the minimum frequency [4, 5]. The VCO should target a tuning sensitivity of 50MHz/V per step across 0-3.3V, power dissipation to be less than 315 mW at 85C and single side band (SSB) phase noise @ 100 kHz offset to be less than -93 dBc/Hz at each center frequency. VCO architecture decisions and semiconductor manufacturing choices must be defended based on the given specifications for this VCO and cost considerations. The study should define the appropriate electronic design automation (EDA) tools for design, simulation, layout and physical verification, and the ability to access these EDA tools. Specifying important semiconductor process parameters, devices and characteristics shall be identified when targeting a semiconductor process. Access to targeted semiconductor processes and their process design kits (PDK's) shall be noted. The challenges and any special considerations for testing this ultra wide-band VCO shall be addressed.

Respondents shall deliver a report that satisfies all of the requirements outlined in Phase I. If any of the above items cannot be fully addressed in the Phase I feasibility report, the report must include relevant research and justification for their inapplicability.

PHASE II: Build, test and deliver a fully functional ultra-wideband VCO prototype based on the design developed in Phase I. Demonstrate the capability over the full range of the selection range while adhering to the specifications outlined in Phase I. Circuit and layout design reviews shall be held to ensure specification compliance and review any tradeoffs. Documentation of circuit and layout reviews shall be delivered. Production yields shall be considered to keep costs low with commercialization a viable option.

PHASE III DUAL USE APPLICATIONS: This technology could be utilized for countless other DoD and commercial communications applications.

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KEYWORDS: Voltage-Controlled Oscillator

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DMEA231-007 TITLE: SiC Stress Tuning

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

OBJECTIVE: Mechanical stress tuning through Finite Element Analysis (FEA) modeling that can be used to predict silicon carbide (SiC) wafer warp/strength through processing steps such as power device fabrication, back grinding, stress relief processing, and backside metallization (BSM).

DESCRIPTION: Stress engineering can be used for structural optimization of power devices, through mechanical stress tuning using FEA to predict stress [5] generated during the various manufacturing processes (dielectric deposition, metal deposition, wafer thinning, and BSM), which enables targeted reduction of stress in processing steps where large amounts of stress are to occur or reduction across multiple processing steps. Reduction of stress at interfaces improves device reliability performance, both in passive and active cycles [5] as well as, improving device yield [1]. Essentially, stress management and its optimization concurrently act as reliability improvement by means of reduction of overall stress, warpage, and a means of piezoresistive characteristics improvement [5]. An immediate effect of piezoresistivity is the change of device drain-source on-state resistance as adequate strain to the substrate is able to reduce Rdson, limiting dissipated power and temperature swing during operational life [5]. FEA has demonstrated the ability to predict wafer warp/strength for silicon (Si) through various fabrication processes.

For front side device fabrication, FEA can be used to estimate the warping behavior of large thin coated wafers from the stress and strain in a thin film layer that is created as a result of either the deposition process or coefficient of thermal expansion (CTE)) mismatch [4]. The intrinsic stress is cause by non-equilibrium growth of the film microstructure, which will vary with the deposition process parameters and the thermal history post deposition [3]. To include front side device patterning in studies increases the complexity of the simulation beyond normal computational limits, but it is estimated that for conductive layers, the stress relief due to patterning is proportional to the area removed [4]. Wafer thinning is done to improve aid sawing operations, improve heat transfer within assemblies, reduce package height, and reduce Rdson [4]. Large warpage, usually as a result of backside processing, is one of the root causes of failures [4]. During wafer thinning, the substrate becomes more fragile, which increases the handling difficulties, as well as creates a potential source of defects that could propagate in subsequent processing steps [4]. As the wafer thickness is decreased during thinning, the wafer progressively become less able to support its own weight and resist the stresses generated by front side dielectric and metal deposition [4]. With a decrease in wafer thickness, the gravitational warp caused by the wafer weight also becomes significant and affects the simulation results if not accounted for [2]. Grinding induces intrinsic compressive stresses from texture disturbance in a subsurface layer [4], which is considered to be proportional to the diamond mesh or grit of the grinding wheel used for processing. Etching or other stress relief methods can be applied to in some cases to completely remove the stresses/subsurface damage caused by back grinding [4].

Lastly, the application of BSM, which acts as a thermal interface between die and package, a bonding layer between die and die attach material, or in some applications, as an electrical interface between die and package. Depending on metal stack materials and layer thickness used, significant wafer deflection can reduce metal adhesion reliability, which in turn, can cause peeling, lower reliability, and lower yield of packaged components. Most studies relate the stress in a film or substrate to the wafer curvature using the Stoney formula, but it has been shown to be inadequate for large deflections where large disagreement has been found [4] and ignores wafer hold mechanics (such as the vacuum holding chuck used in wafer thinning) [2]. The Stoney formula is also not comprehensive enough to analyze wafer saddle shaped warpage (structures warped with compound curvature) [1]. Furthermore, for wafers of which thickness was reduced to less than 200microns, wafer warp became more severe and could be large in the elastic

range or even beyond rendering the superposition method null to the calculation of the total warp [2]. Ultimately, the application of information learned from research on predictive modeling of silicon wafers could be combined and translated to build a parameterized system [2] that can be used by process engineers, without strong FEA knowledge, to examine and optimize both front side deposition, backside grind, and BSM processes used in the fabrication of high voltage SiC devices.

The optimal solution will approach or exceed the following performance metrics:

1. Front side fabrication model/simulation shall include a device with up to two metal layers minimum
    a. For a given metal layer approximate surface area range of 10-50% must be shown
    b. Metal layers shall cover a thickness of 1000-3000Angstoms
2. Back grinding shall include at least two different grit sizes used in grinding wheels with diamond mesh sizes associated with fine grinding and coarse grinding
    a. Input for final (post thinning) thickness of substrate must include at minimum: 100um, 150um, 200um, 250um, and 300um
3. Wafers thinned to various thickness under the different grinding conditions represented in the study
4. BSM should include metal stacks of Ag/Au/Ni and Ti/Ni/Ag
    a. Two different metal thicknesses (on order of .1um to 5um) for each metal layer for each stack
5. Predicted results accurate to 5%
6. Able to receive input from user to flag/warn if stress or strength is not within acceptable limits provided by user

PHASE I: Perform a feasibility study on the ability to utilize FEA or other computation means to predict the SiC wafer warpage and in turn, the residual stress in the wafer from power device fabrication, taking into account the effects of each processing step (front side deposition, backside grinding and BSM) and the processing parameters used during manufacturing. Develop a means in which engineers without FEA knowledge could input processing parameters for the aforementioned manufacturing steps to output a resultant warpage prediction and the associated residual stress.

PHASE II: From the study prepared in Phase I, perform development of the prototype architecture of the predictive tool and experimental verification of the tool to predict warp and stress across a SiC wafer processed through front side fabrication, including deposition of dielectric materials and metals, back grinding, and BSM deposition. The performer is expected to show repeatability in the simulation performed and in the experiments performed as part of the verification of the tool, as well as deliver the testing data and the samples for which the experiments were executed.

PHASE III DUAL USE APPLICATIONS: Predictive simulation tool or analysis capability can be marketed toward industry for commercial application and DoD for unique or low volume device manufacturing to use to support product design for cost and risk reduction as well as, design and reliability optimization.

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KEYWORDS: Silicon carbide, Backside metal deposition, back grinding, stress engineering

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DMEA231-008 TITLE: Automated Measurement of Passive Devices in Printed Circuit Assemblies

OUSD (R&E) CRITICAL TECHNOLOGY AREA(S): Microelectronics

OBJECTIVE: Design and implement a system that would automate the measurement of passive electronic components (capacitors, inductors, and resistors). The components can be measured in place or removed and measured in an automated fashion.

DESCRIPTION: Manual measurement of passive devices requires a large amount of human resources to complete, involving handling of small components and manual measurement techniques, which are labor intensive and prone to human error. Automation of this process would reduce manual steps resulting in faster throughput, improved accuracy, and reduced risk of data loss for reverse engineering applications where samples may be limited or irreplaceable. The Defense Microelectronics Activity (DMEA) is interested in an automated solution for the measurement of passive devices (resistors, capacitors, and inductors) [1, 2, 4]. A system which can perform these functions does not currently exist in the marketplace. The system may utilize DMEA's in house automated flying pin prober as a potential solution [3]. Applications for an automated measurement solution for passive devices on printed circuit board (PCB) include reverse engineering of near obsolescent equipment for the creation of technical data packages, automation of general counterfeit detection, and verification of manufactured solutions for quality assurance purposes [3, 4].

Requirements of the tool are as follows:

1. A tool which can achieve 99% size and electrical characteristic measurement accuracy of 95% of all surface mount technology capacitors, inductors, and resistors of standard package types ranging from 01005 (.4mm X .2mm) through 2920 (7.5mm X 5.1mm) from a PCB assembly used in high frequency communications application of medium to high circuit density.
2. For those devices that cannot be measured accurately in place, identify a method of flagging which components will have to be measured manually. It is essential that the operator know which of the measurements are outside of the tools range, so that follow up measurement can be performed for accurate results.
3. Tool chamber should be suitable to accept electrostatic discharge (ESD) sensitive PCBs up to 12-inch by 12-inch dimensions.

PHASE I: Conduct research to design tool that can identify and measure passive components (capacitors, inductors, and resistors) on printed circuit assemblies. The tool may remove components in an automated way and then measure them, measure them in place, or some combination of the two approaches. For in-place measurement solutions, it can assumed that the layout of the PCB can be acquired separately and traces connecting the target component may be severed if necessary. The end product of Phase I is a feasibility study report, in which the following must be specified:

1. A clear description of how the tools works.
2. Total cost of the tool including installation and operator training.
3. Maintenance requirements.
4. A clear description of facilitation of the tool (power requirements, clean dry air, cooling, etc.)
5. Skill level or special training requirements for the operator of the tool.
6. Limitations on automated measurements (for example, component sizes, component types or values, component layouts, etc.).
7. What information is required as input?
8. What if any manual steps are still required?

PHASE II: Develop a prototype of the Phase I concept and demonstrate its operation. Validate the performance in a way that realistically demonstrates how the technology would be deployed. This demonstration will include scalability of the technology in terms of capacity, accuracy, cost, and time.

PHASE III DUAL USE APPLICATIONS: There may be opportunities for further development of this innovation for use in a specific military or commercial application. During Phase III, the contractor may refine the performance of the design and produce pre-production quantities for evaluation by the Government. The proposed technology will be applicable to both commercial and government fields for analysis of printed circuit assemblies. Government applications include reverse engineering, automation of general counterfeit detection, and failure analysis of printed circuit card assemblies. Commercial applications could include verification of printed circuit assemblies and validation of manufacturing processes.

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KEYWORDS: Reverse engineering, Technical Data Package, Test and Measurement of Passive Devices, Microelectronics, PCB automation, Anti-Counterfeit

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